Assignment-2

Embedded System

1. Define the following precisely and contrast them in 2–3 lines each: instruction cycle, machine cycle, T-state, and control/status signals (ALE, RD, WR, IO/M, S1, S0). Explain how these combine to represent an instruction's temporal behavior.
2. List the five fundamental machine cycles of 8085 and state the typical T-state count for each. Explain why the opcode fetch cycle usually takes more T-states than a memory read cycle.
3. Describe the role of ALE during T1 in any memory-accessing cycle. How does bus multiplexing (AD7–AD0) influence the sequence of events across T1–T3?
4. For each machine cycle (Opcode Fetch, Memory Read, Memory Write, I/O Read, I/O Write), specify:
    - IO/M, S1, S0 levels
    - Whether ALE goes high, and in which T-state
    - When RD/WR are asserted and de-asserted
    - What is on AD7–AD0 in T1 vs. later T-states
5. Compute total T-states for each instruction and break down by machine cycles:

    MOV B, C
    MOV M, A
    MVI M, 55H
    LDA 4030H
    STA 2000H
    LHLD 8050H
    XTHL
    IN 80H
    OUT 01H
    PUSH PSW, POP PSW
    CALL 2400H, RET