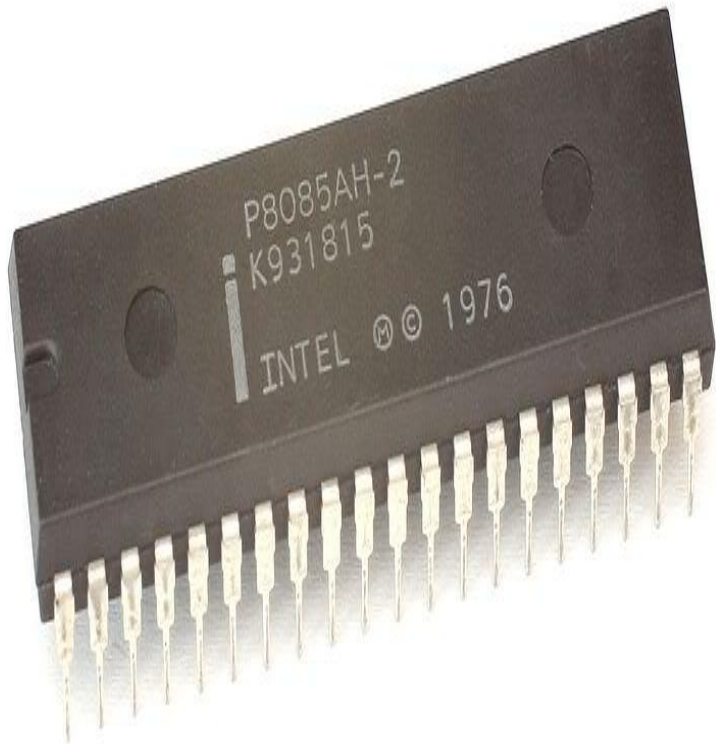


Introduction to 8085

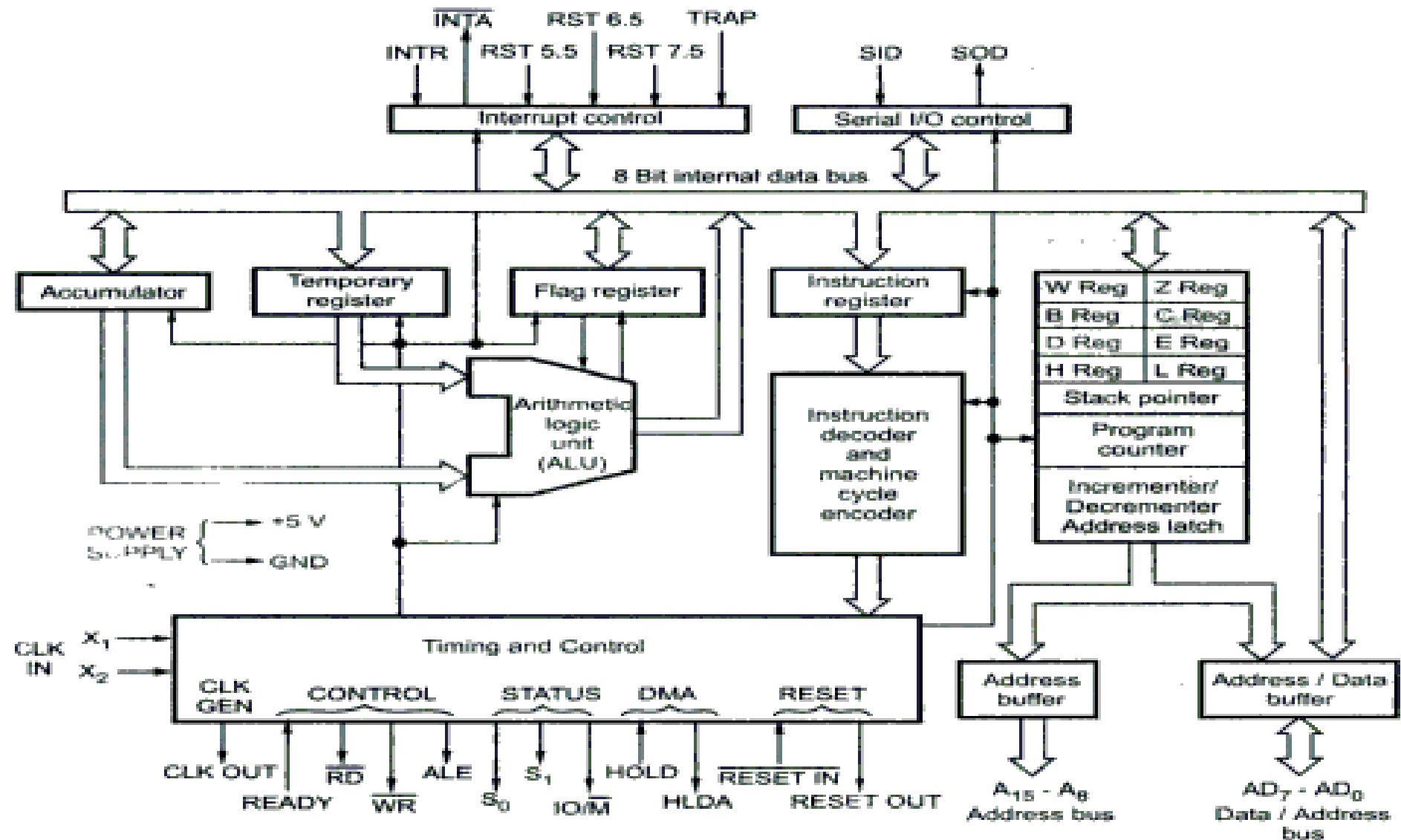


- Introduced in 1977.
- It is 8-bit MP.
- It is a 40 pin dual-in-line chip.
- It uses a single +5V supply for its operations.
- Its clock speed is about 3MHz.

Features of 8085

- It is manufactured with N-MOS technology.
- It has 16-bit address bus and hence can address up to $2^{16} = 65536$ bytes (64KB) memory locations through A0 - A15.
- The first 8 lines of address bus and 8 lines of data bus are multiplexed AD0 – AD7.
- Data bus is a group of 8 lines D0 – D7 .
- It supports external interrupt request.
- A 16 bit program counter (PC)
- A 16 bit stack pointer (SP)
- Six 8-bit general purpose registers arranged in pairs: BC, DE, HL.

8085 Architecture



Intel 8085 Microprocessor

- 8085 consists of:
 - **Control unit:** control microprocessor operations.
 - **ALU:** performs data processing function.
 - **Registers:** provide storage internal to CPU.
 - **Interrupts**
 - **Internal data bus**

8085 Architecture Contd..

- **ALU – Arithmetic & Logic Unit**
 - ALU of 8085 performs 8-bit arithmetic & logical operations. The operations are generally performed with Accumulator as one of the operands. The result is saved in accumulator register.
- **Timing & Control Unit**
 - This unit works as the brain of the CPU and generates all the timing and control signals to perform all the internal & external operations of the CPU.
- **Instruction Decoder & Machine Cycle Encoder Unit**
 - This unit decodes the op-code stored in the Instruction Register (IR) and encodes it for the timing & control unit to perform the execution of the instruction.

8085 Architecture Contd..

- The Registers are of 8-bit & 16-bit size used for different purposes
 - **A- Accumulator** - This is an special purpose register. All the ALU operations are performed with reference to the contents of Accumulator.
 - **B,C,D,E,H,L** - General purpose registers. These registers can also be used for 16-bit operations in pairs. The default pairs are BC, DE & HL.
 - **F – Flag register** - This register indicates the status of the ALU operation.
 - **PC – Program Counter** - This is a 16-bit register used to address the memory location from where an instruction is going to be executed.
 - **SP – Stack pointer** - This is a 16-bit register used to address the top of the stack memory location.
 - **Temp. register, W & Z** - These registers are only used by 8085 and are not available for the programmer.

8085 Architecture Contd..

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Arithmetic & Logic Unit (ALU)

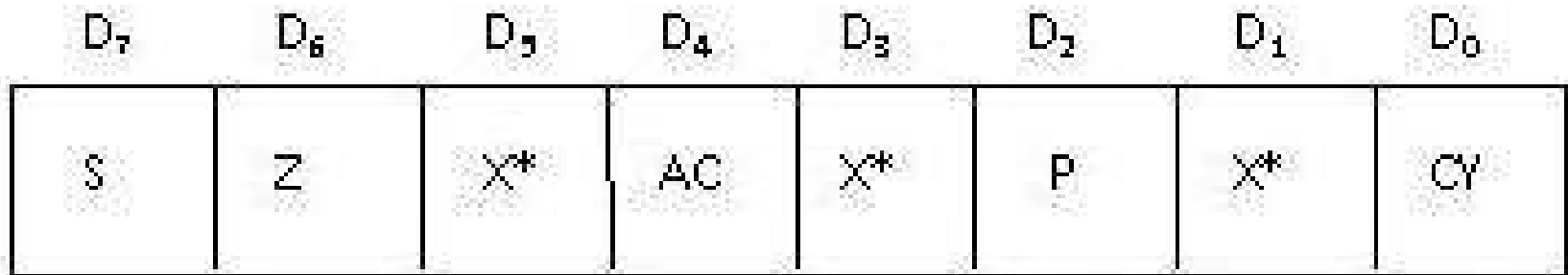
- It performs various arithmetic and logic operations.
- The data is available in accumulator and temporary/general purpose registers.
- **Arithmetic Operations:**
 - Addition, Subtraction, Increment, Decrement etc.
- **Logic Operations:**
 - AND, OR, X-OR, Complement etc.

Accumulator

- It the main register of microprocessor.
- It is also called register 'A'.
- It is an 8-bit register.
- It is used in the arithmetic and logic operations.
- It always contains one of the operands on which arithmetic/logic has to be performed.
- After the arithmetic/logic operation, the contents of accumulator are replaced by the result.

The Flags Register - Status Flags

- Status Flags are set of flip-flops which are used to check the status of Accumulator after the operation is performed.



X* = don't care condition

The Flags register

- There is also a flag register whose bits are affected by the arithmetic & logic operations.
 - **S-sign flag**
 - The sign flag is set if bit D7 of the accumulator is set after an arithmetic or logic operation.
 - **Z-zero flag**
 - Set if the result of the ALU operation is 0. Otherwise is reset. This flag is affected by operations on the accumulator as well as other registers. (DCR B).
 - **AC-Auxiliary Carry**
 - This flag is set when a carry is generated from bit D3 and passed to D4 . This flag is used only internally for BCD operations.
 - **P-Parity flag**
 - After an ALU operation, if the result has an even # of 1s, the p-flag is set. Otherwise it is cleared. So, the flag can be used to indicate even parity.
 - **CY-carry flag**
 - This flag is set when a carry is generated from bit D7 after an unsigned operation.
 - **OV-Overflow flag**
 - This flag is set when an overflow occurs after a signed operation.

Status Flags

- The flags are stored in the 8-bit register so that the programmer can examine these flags (data conditions) by accessing the register through an instruction.
- These flags have critical importance in the decision-making process of the microprocessor.
- The conditions (set or reset) of the flags are tested through the software instructions.
- For example, the instruction JC (Jump on Carry) is implemented to change the sequence of a program when CY flag is set.

Status Flags

- S = Sign Flag
- Z = Zero Flag
- AC = Auxiliary Carry Flag
- P = Parity Flag
- CY = Carry Flag

Status Flags

- **Sign Flag (S):**
 - Used for indicating the sign of the data in the accumulator
 - The sign flag is set if negative (1 –negative)
 - The sign flag is reset if positive (0 –positive)

Status Flags

- **Auxiliary Carry Flag (AC):**
 - It is used in BCD operations.
 - When there is carry in BCD addition, we add 0110 (6) to the result.
 - If there is carry in BCD addition, auxiliary carry is set (1).
 - If there is no carry, auxiliary carry is reset (0).

Status Flags

- **Parity Flag (P):**
 - Is set(1) if the parity (the number of set bits in the result) is even.
 - Is cleared(0) if parity is odd.

Status Flags

- **Carry Flag (CY):**

- Is set if there is a carry or borrow from arithmetic operation (carry during addition/rotation, or borrow during subtraction/comparison)

```
  1011 0101
+ 0110 1100
-----
```

Carry 1 0010 0001

```
  1011 0101
- 1100 1100
-----
```

Borrow 1 1110 1001

- **Zero Flag (Z):**

- Is set if result obtained after an operation is 0.
- Is set following an increment or decrement operation of that register

```
    10110011
+   01001101
-----
  1 00000000
```

Temporary Register

- It is an 8-bit register.
- It is used to store temporary 8-bit operand from general purpose register.
- It is also used to store intermediate results.
- The programmer can not access this register. However, it is internally used for execution of most of the ALU operations.

Instruction Register/Decoder

- The opcode of instruction fetched from memory and stored in the instruction register. (Temporary store for the current instruction of a program).
- Decoder then takes instruction and “decodes” or interprets the instruction. Decoded instruction then passed to next stage.
- Accordingly it gives the timing and control signals
 - which control the registers, data buffer, ALU and external peripheral signals depending on the nature of instruction.

Timing and Control Unit

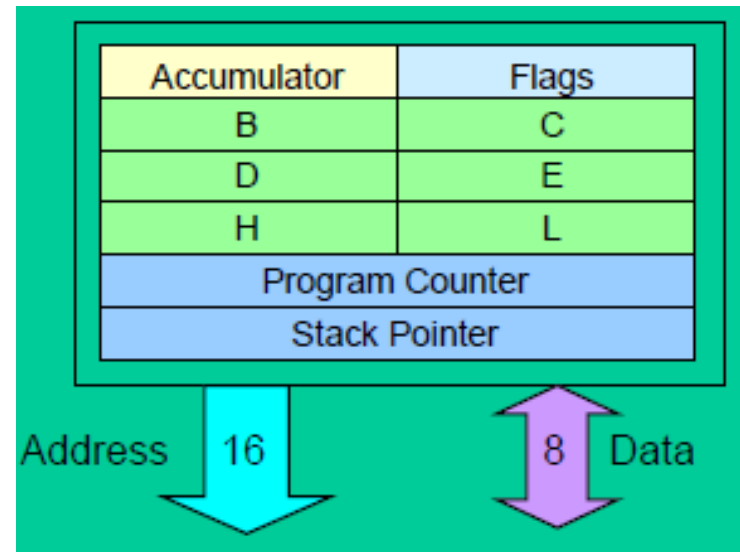
- It controls all the operations of microprocessor and peripheral devices.
- Depending upon the machine cycles received from Instruction Decoder, it generates control signals:
 - S0 and S1 (Status Signals).
 - ALE (Address Latch Enable).
 - RD (Read, active low).
 - WR (Write, active low).

Timing and Control Unit

- IO/M (Input-Output/Memory).
- READY
- RESET IN
- RESET OUT
- CLK OUT
- HOLD and HLDA

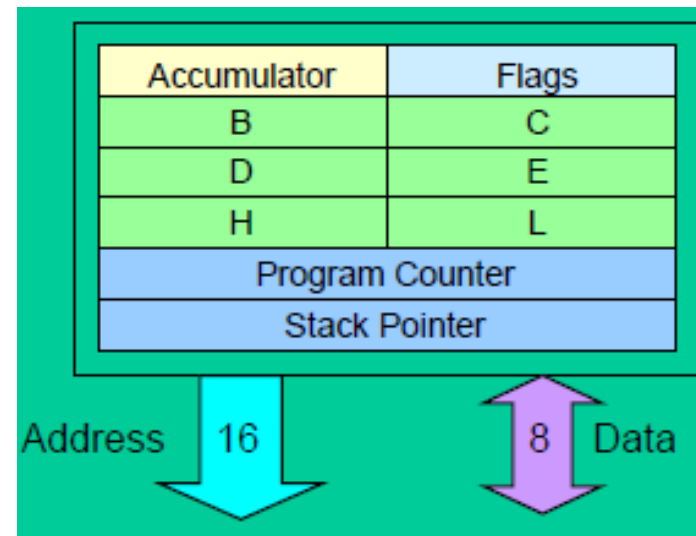
General Purpose Registers

- B, C, D, E, H& L(8 bit registers)
- Can be used singly
- Or can be used as 16 bit register pairs
 - BC, DE, HL
- H & L can be used as a data pointer
(holds memory address)



General Purpose Registers

- General Purpose Registers
 - B, C, D, E, H& L(8 bit registers)
 - Can be used singly
 - Or can be used as 16 bit register pairs
 - BC, DE, HL
 - H & L can be used as a data pointer (holds memory address)
- Special Purpose Registers
 - Accumulator(8 bit register)
 - Store 8 bit data
 - Store the result of an operation
 - Store 8 bit data during I/O transfer



Program Counter

- It is used to hold the address of next instruction to be executed.
- It is a 16-bit register.
- The microprocessor uses this register to sequence the execution of the instructions.
- The microprocessor increments the value of Program Counter after the execution of the current instruction, so that, it always points to the next instruction.

Stack Pointer

- It holds the address of top most item in the stack. The stack is a reserved area of memory in the RAM
- It is also 16-bit register.
- Any portion of memory can be used as stack.
- This register is always decremented/incremented by 2 during push and pop.
- The stack is usually accessed in a Last In First Out (LIFO) fashion.

Increment/Decrement Register

- This register is used to increment or decrement the value of Stack Pointer or program counter as a part of execution of instructions.
- During PUSH operation, the value of Stack Pointer is incremented.
- During POP operation, the value of Stack Pointer is decremented.

Address Latch

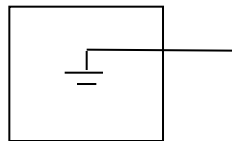
- It is a unidirectional 8-bit buffer.
- The upper-byte of 16-bit address is stored in this latch. And then it is made available to the peripheral devices.
- It is used to drive external high order address bus(A15-A0).
- It is also used to tri-state the high order address bus under certain conditions such as
 - Reset, hold, halt and when address lines are is not in use.

Address/Data Latch

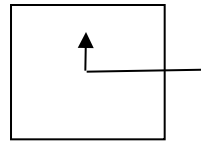
- The lower-byte of address and 8-bit of data are multiplexed.
- It holds either lower-byte of address or 8-bits of data.
- This is decided by ALE (Address Latch Enable) signal.
 - If ALE = 1 then
 - Address/Data Latch contains lower-byte of address.
 - If ALE = 0 then
 - It contains 8-bit data.

Tri-State Buffers

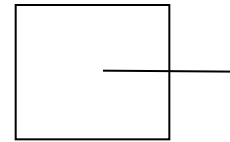
- An important circuit element that is used extensively in memory.
- This buffer is a logic circuit that has three states:
 - Logic 0, logic1, and high impedance.
 - When this circuit is in high impedance mode it looks as if it is disconnected from the output completely.



The Output is Low



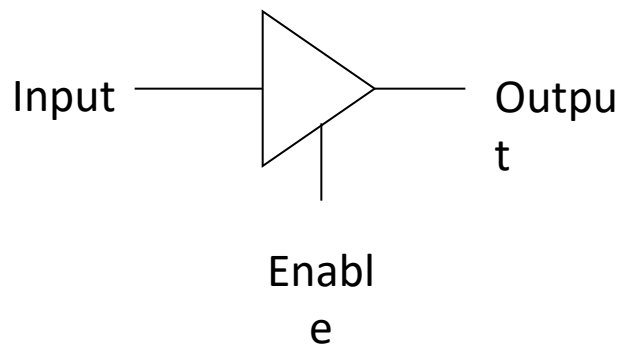
The Output is High



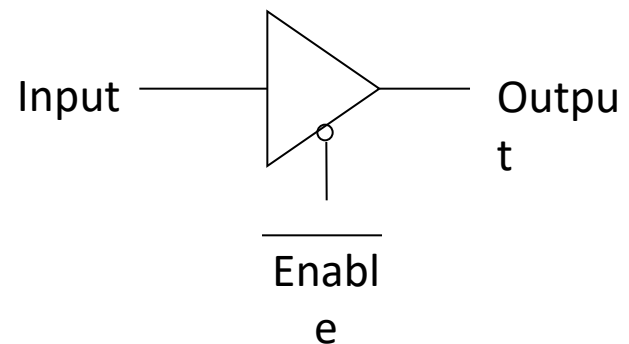
High Impedance

The Tri-State Buffer

- This circuit has two inputs and one output.
 - The first input behaves like the normal input for the circuit.
 - The second input is an “**enable**”.
 - If it is set high, the output follows the proper circuit behavior.
 - If it is set low, the output looks like a wire connected to nothing.



OR



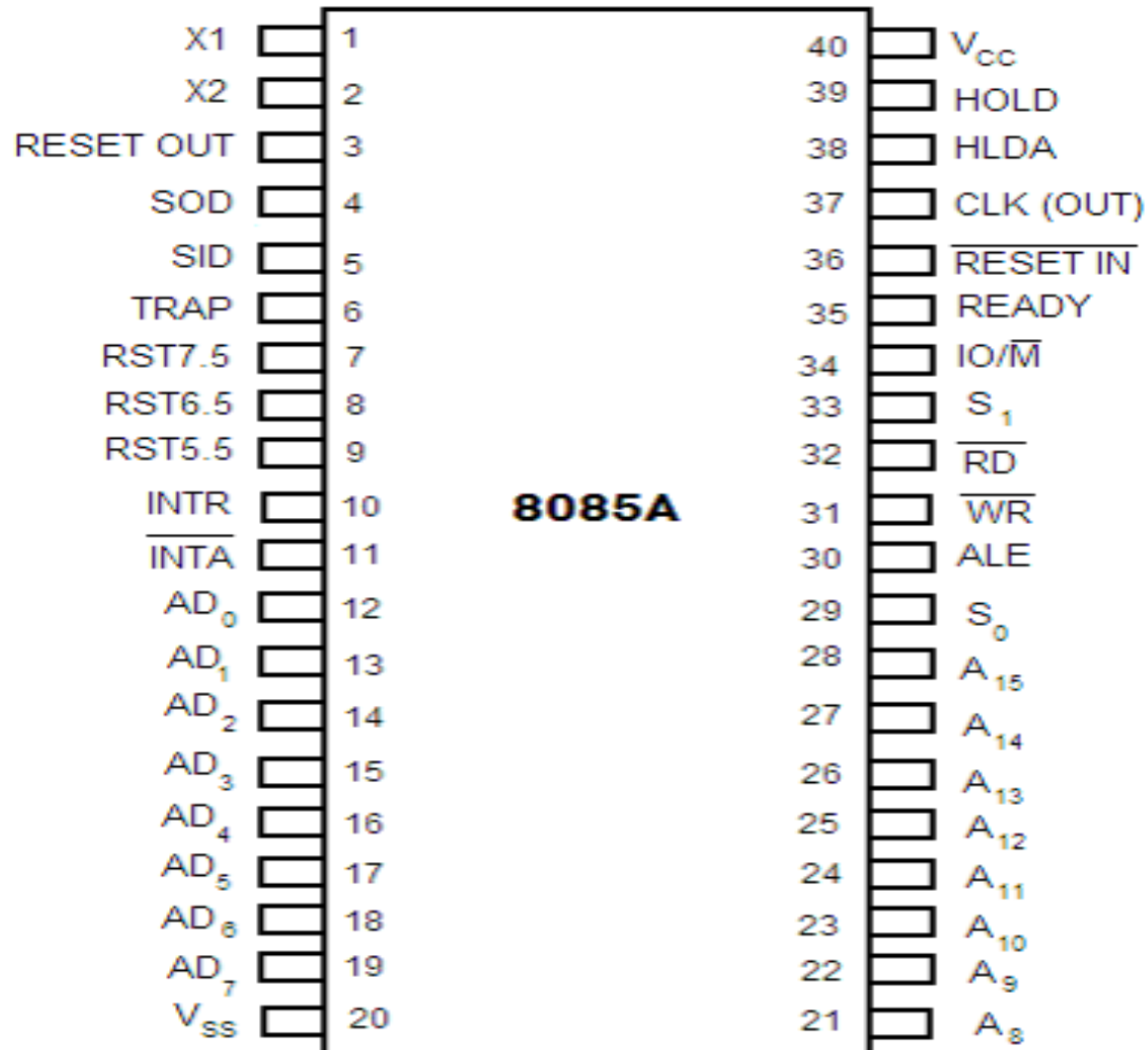
Serial I/O Controller

- It is used to convert parallel data into serial.
- Microprocessor works with 8-bit parallel data.
- Serial I/O devices works with serial transfer of data.
- Therefore, this unit is the interface between microprocessor and serial I/O devices.

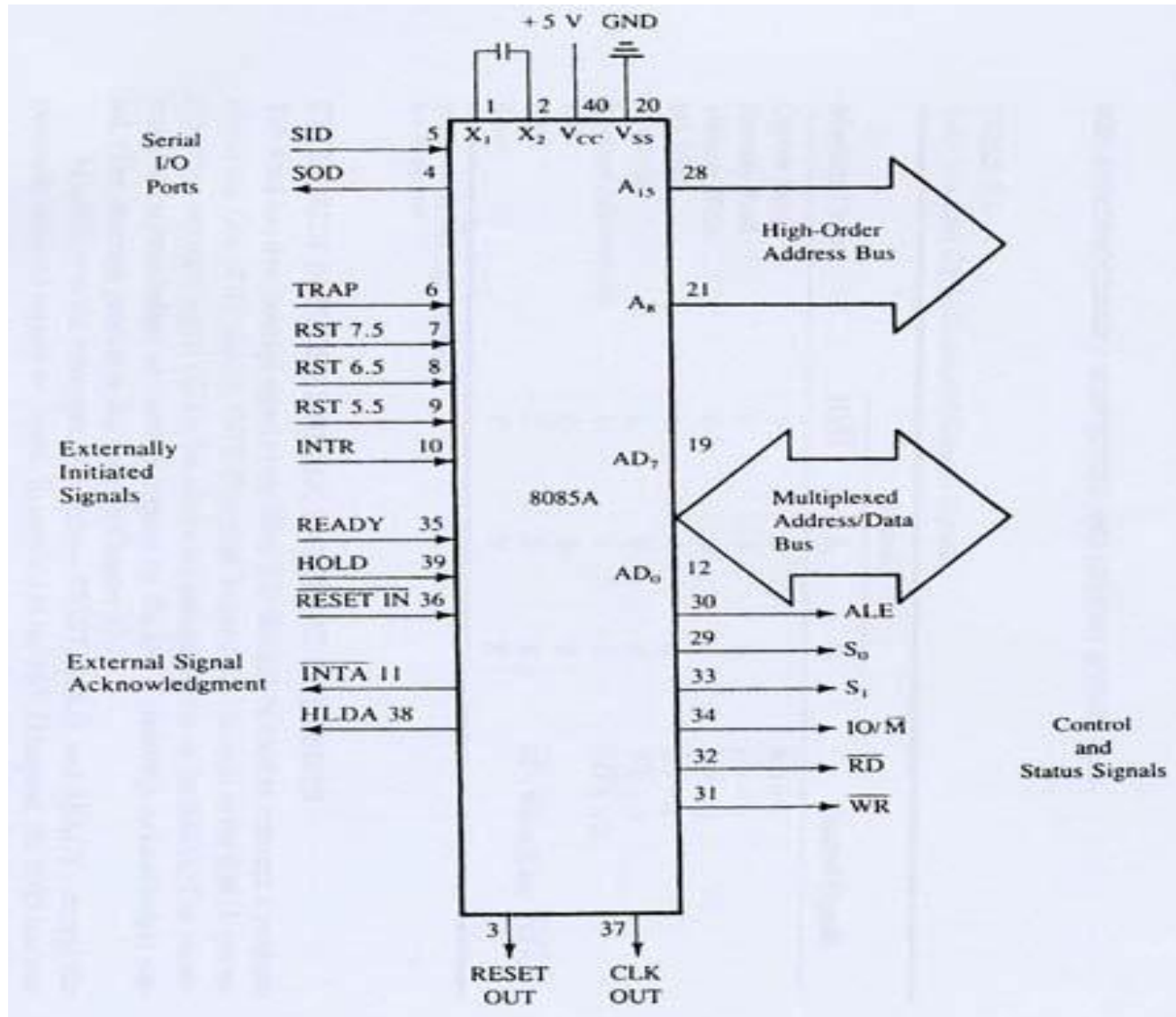
Interrupt Controller

- It is used to handle the interrupts.
- There are 5 interrupt signals in 8085:
 - TRAP
 - RST 7.5
 - RST 6.5
 - RST 5.5
 - INTR
- Interrupt controller receives these interrupts according to their priority and applies them to the microprocessor.
- There is one outgoing signal INTA which is called Interrupt Acknowledge.

Pin Diagram of 8085



Pin description of 8085



Pin description

- Higher Order Address pins- $A_{15} - A_8$
- Lower Order Address/ Data Pins- AD_7-AD_0
 - These are time multiplexed pins and are de-multiplexed using the pin ALE
- Control Pins – RD, WR
 - These are active low Read & Write pins
- Status Pins – ALE, IO/M (active low), S_1, S_0
 - ALE (Address Latch Enable)-Used to de-multiplex AD_7-AD_0
 - IO/M – Used to select I/O or Memory operation
 - S_1, S_0 – Denote the status of data on data bus
- Interrupt Pins – TRAP, RST7.5, RST 6.5, RST 5.5, INTR, INTA
 - These are hardware interrupts used to initiate an interrupt service routine stored at predefined locations of the system memory.
- Serial I/O pins – SID (Serial Input Data), SOD (Serial Output Data)
 - These pins are used to interface 8085 with a serial device.

Pin Description

Contd...

- **Clock Pins- X_1 , X_2 , CLK(OUT)**
 - X_1 , X_2 - These are clock input pins. A crystal is connected between these pins such that $f_{\text{crystal}} = 2f_{8085}$ where f_{crystal} = crystal frequency & f_{8085} = operating frequency of 8085
 - CLK(OUT) – This is an auxiliary clock output source
- **Reset Pins – Reset In (active low), Reset Out**
 - **Reset In** is used to reset 8085 whereas **Reset Out** can be used to reset other devices in the system
- **DMA (Direct Memory Access) pins – HOLD, HLDA**
 - These pins are used when data transfer is to be performed directly between an external device and the main memory of the system.
- **Power Supply Pins - $+V_{CC}$, V_{SS}**

The 8085 and Its Buses

- The 8085 is an **8-bit general purpose** microprocessor that can address **64K Byte of memory**.
- It has **40 pins** and uses +5V for power. It can run at a **maximum frequency of 3 MHz**.
 - The pins on the chip can be grouped into 6 groups:
 - **Address Bus.**
 - **Data Bus.**
 - **Control and Status Signals.**
 - **Power supply and frequency.**
 - **Externally Initiated Signals.**
 - **Serial I/O ports.**

The Address and Data Busses

- The address bus has 8 signal lines **A8 – A15** which are **unidirectional**.
- The other 8 address bits are **multiplexed** (time shared) **with the 8 data bits**.
 - So, the bits **AD0 – AD7** are **bi-directional** and serve as **A0 – A7** and **D0 – D7** at the same time.
 - During the execution of the instruction, these lines carry the address bits during the early part, then during the late parts of the execution, they carry the 8 data bits.
 - In order to separate the address from the data, we can use a latch to save the value before the function of the bits changes.

The Control and Status Signals

- There are 4 main **control** and **status** signals. These are:
- **ALE: Address Latch Enable.**
 - This signal is a pulse that become **1** when the **AD0 – AD7** lines have an **address** on them. It becomes 0 after that. This signal can be used to enable a latch to save the address bits from the AD lines.
- **RD: Read. Active low.** - Read memory or IO device.
 - This indicates that the selected memory location or I/O device is to be read and that the data bus is ready for accepting data from the memory or I/O device
- **WR: Write. Active low.** - Write memory or IO device.
 - This indicates that the data on the data bus is to be written into the selected memory location or I/O device.
- **IO/M:** Select memory or an IO device.
 - This signal specifies whether the operation is a **memory operation** (**IO/M=0**) or an **I/O operation** (**IO/M=1**).
 - It goes high to indicate an I/O operation.
 - It goes low for memory operations.
- **S1 and S0 :** Status signals
 - to specify the **kind of operation** being performed.
 - This status signal indicates that the read / write operation relates to whether the memory or I/O device.

Status Signals(S1 and S0)

- It is used to know the type of current operation of the microprocessor.

IO/M	S1	S0	OPERATION
0	1	1	Opcode fetch
0	1	0	Memory read
0	0	1	Memory write
1	1	0	I/O read
1	0	1	I/O write
1	1	0	Interrupt acknowledge
Z	0	1	Halt
Z	x	x	Hold
Z	x	x	Reset

Power supply and Clock frequency signals:

- **Vcc:** + 5 volt power supply
- **Vss:** Ground
- **X1, X2 :**
 - Crystal or R/C network or LC network connections to set the frequency of internal clock generator. The frequency is internally divided by two. Since the basic operating timing frequency is 3 MHz, a 6 MHz crystal is connected externally.
- ***CLK (Output)***
 - Clock Output is used as the system clock for peripheral and devices interfaced with the microprocessor.

Frequency Control Signals

- There are **3** important pins in the frequency control group.
 - **X0** and **X1** are the **inputs** from the **crystal** or clock generating circuit.
 - The frequency is internally divided by 2.
 - So, to run the microprocessor at 3 MHz, a clock running at 6 MHz should be connected to the X0 and X1 pins.
 - **CLK (OUT)**: An output clock pin to drive the clock of the rest of the system.
- We will discuss the rest of the control signals as we get to them.

The 8085 Interrupts

- The 8085 has 5 interrupt inputs.
 - The INTR input.
 - The INTR input is the only **non-vector** interrupt.
 - INTR is **maskable** using the EI/DI instruction pair.
 - RST 5.5, RST 6.5, RST 7.5 are all **automatically vectored**.
 - RST 5.5, RST 6.5, and RST 7.5 are all **maskable**.
 - TRAP is the only **non-maskable** interrupt in the 8085
 - TRAP is also **automatically vectored**

Interrupt Signals

- 8085 μ p has several interrupt signals as shown in the following table.

TABLE 4.2

8085 Interrupts and Externally Initiated Signals

<input type="checkbox"/> INTR (Input)	Interrupt Request: This is used as a general-purpose interrupt; it is similar to the INT signal of the 8080A.
<input type="checkbox"/> $\overline{\text{INTA}}$ (Output)	Interrupt Acknowledge: This is used to acknowledge an interrupt.
<input type="checkbox"/> RST 7.5 (Inputs) RST 6.5 RST 5.5	Restart Interrupts: These are vectored interrupts that transfer the program control to specific memory locations. They have higher priorities than the INTR interrupt. Among these three, the priority order is 7.5, 6.5, and 5.5.
<input type="checkbox"/> TRAP (Input)	This is a nonmaskable interrupt and has the highest priority.
<input type="checkbox"/> HOLD (Input)	This signal indicates that a peripheral such as a DMA (Direct Memory Access) controller is requesting the use of the address and data buses.
<input type="checkbox"/> HLDA (Output)	Hold Acknowledge: This signal acknowledges the HOLD request.
<input type="checkbox"/> READY (Input)	This signal is used to delay the microprocessor Read or Write cycles until a slow-responding peripheral is ready to send or accept data. When this signal goes low, the microprocessor waits for an integral number of clock cycles until it goes high.

Serial communication Signal

- **SID - Serial Input Data Line:**
 - The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
- **SOD – Serial Output Data Line:**
 - The SIM instruction loads the value of bit 7 of the accumulator into SOD latch if bit 6 (SOE) of the accumulator is 1.

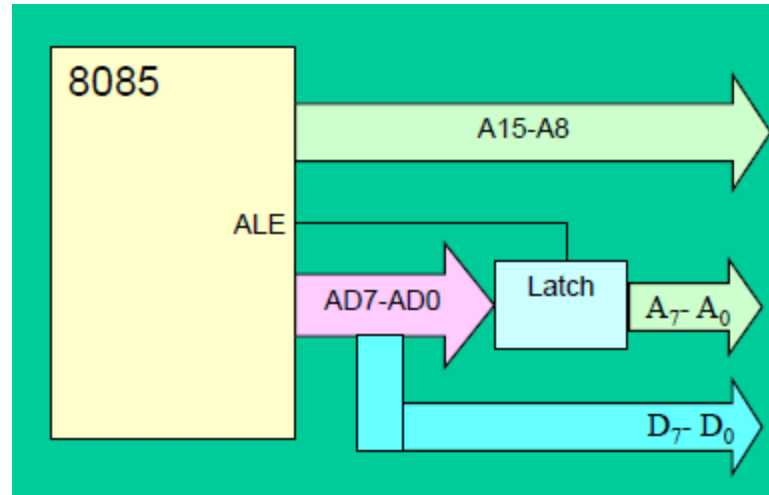
Reset signals

- **Reset In (input, active low)**
 - This signal is used to reset the microprocessor.
 - The program counter inside the microprocessor is set to zero.
 - The buses are tri-stated.
- **Reset Out (Output)**
 - It indicates CPU is being reset.
 - Can be used as a system RESET. The signal is synchronized to the processor clock.
 - Used to reset all the connected devices when the microprocessor is reset.

Demultiplexing AD7-AD0

- From the above description, it becomes obvious that the AD7–AD0 lines are serving a **dual purpose** and that they need to be demultiplexed to get all the information.
- The **high order bits** of the address remain on the bus for **three clock periods**. However, the **low order bits** remain for only one clock period and they would be lost if they are not saved externally. Also, notice that the **low order bits** of the address disappear when they are needed most.
- To make sure we have the entire address for the full three clock cycles, we will use **an external latch** to save the value of AD7–AD0 when it is carrying the address bits. We use the **ALE** signal to enable this latch.

Demultiplexing AD7-AD0



- Given that ALE operates as a pulse during T1, we will be able to latch the address. Then when ALE goes low, the address is saved and the AD7-AD0 lines can be used for their purpose as the bi-directional data lines.

Demultiplexing the Bus AD7–AD0

- The high order address is placed on the address bus and hold for 3 clk periods,
- The low order address is lost after the first clk period, this address needs to be hold however we need to use latch
- The address AD7 –AD0 is connected as inputs to the latch 74LS373.
- The ALE signal is connected to the enable (G) pin of the latch and the OC –Output control –of the latch is grounded

