Rajiv Gandhi Institute of Petroleum Technology, Jais, Amethi

B.Tech-3rd Year (CSE+IDD+IT+MNC)

Odd Semester Mid-Semester Examination, AY: 2024-25

Subject: CS321 Theory of Computation

Date and Time: 04/10/2024, 12:00 PM to 2:00 PM **Total Marks:30**

Instructions:

i) There are 8 questions in this question paper.

ii) You have to attempt all the questions.

iii) Marks against each question are indicated in big brackets.

iv) Attempt the questions in serial order (if possible).

1. The complement of a context-free language is always context-free. Prove your answer using formal methods and examples. [4]

2. Determine if the language $L=\{w \mid w \in \{a,b\}^*$, the number of a's in w is equal to the number of b's$\}$ is context-free or regular. Justify your answer with a formal argument. [4]

3. Design a Moore machine that outputs 1 if the binary input string contains an even number of 1s and outputs 0 otherwise. Clearly specify the state transition diagram, state table, and the corresponding output function. [4]

4. A popular e-commerce website needs to validate discount codes entered by users during checkout. Each valid discount code must adhere to the following rules: [2+2]

- It must start with exactly two uppercase letters (A-Z).
- Followed by any combination of digits (0-9) or lowercase letters (a-z), with a minimum of 3 and a maximum of 5 characters.
- The discount code can end with either a single exclamation mark ! or the sequence $$.

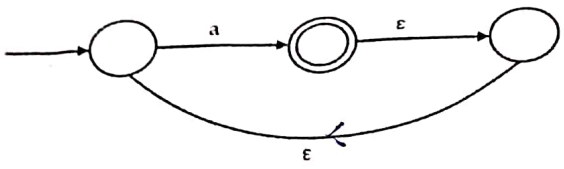
Part 1:

Model this problem using a deterministic **finite automaton (DFA)** that accepts all valid discount codes. Clearly describe the states, transitions, and final states of your automaton.

Part 2:

Write a **regular expression** that represents the set of valid discount codes described above.

Q.5 Find the complement of the language accepted by the NFA shown below? Assume $\Sigma = \{a\}$ and ε is the empty string: [2]



Q.6 A network security company is building a firewall to detect and block malicious URL patterns that hackers use to bypass filters. The company needs to ensure that only valid URLs pass through. URLs are valid if they follow this pattern:

The domain part of the URL contains repeated patterns of "www" followed by alphanumeric characters (e.g., wwwabc123wwwxyz456).

To detect malicious URLs, you want to block any URLs where the domain part contains a string that has a repeated pattern exceeding a certain threshold (indicating a suspicious repetition). However, the company encounters a specific type of malicious URL where the domain consists of excessive repetition of "www" followed by any string, for example:

wwwxxxwwwxxxwwwxxxwwwxxxwwwxxxwwwxxxwwwxxx... (repeating "www" followed by a three-character string).

Prove that the language of these malicious URLs cannot be recognized by any finite automaton using the **pumping lemma for regular languages**. Assume the malicious URL domain is of the form $L=\{(wwwxyz)^n \mid n\geq 1\}$ where xyz represents any combination of letters or numbers. [4]

Q.7 Construct a PDA for the language $L=\{a^n b^{n+1} \mid n\geq 0\}$. Can this language be accepted by a deterministic PDA (DPDA)? If yes, provide the DPDA, and if not, explain why a DPDA cannot handle this language. [4]

Q.8. Compare and contrast the power of DPDAs and NPDAs. Are there languages that can be accepted by an NPDA but not by a DPDA? Provide an example and explanation. [4]

ODD Semester, Mid Term Examination

Subject: - Embedded System (EC E325) MM 30

Date: 27-09-24 (Friday) Time: 12 PM – 2 PM

NOTE: ALL ANSWERS MUST BE WRITTEN ON THE ANSWER SHEET WITH PROPER JUSTIFICATION. ANY KIND OF OVERWRITING WILL RESULT IN ZERO OR NEGATIVE MARKS.

SECTION-I [10 MARKS]

Multiple options may be correct out of four options provided. Carry **TWO** mark each.

FOR EVERY INCORRECT 2-MARK QUESTION, 1 MARKS ARE DEDUCTED

Q1. Which of the following statements about the Analog Input (ADC) on an mbed microcontroller are correct?
a) The ADC can be used to measure voltage levels from sensors. **b)** The resolution of the ADC determines the number of discrete values it can output. **c)** ADC conversion time is typically fixed and does not vary with input signal changes. **d)** The ADC is used to convert digital signals into analog outputs.

Q2. A DAC on an mbed microcontroller has a 10-bit resolution and operates with a reference voltage of 5V. Which of the following are true about the DAC output?
a) The DAC can produce 1,024 discrete voltage levels. **b)** The voltage step size of the DAC is 4.88 mV. **c)** The DAC can output a maximum voltage of 5V. d) The DAC can represent an analog voltage range from 0V to 10V.

Q3. Consider a PWM signal with a frequency of 1 kHz and a duty cycle of 25%. Which of the following statements are correct?
a) The period of the PWM signal is 1 millisecond. **b)** The signal is HIGH for 250 microseconds during each period. **c)** The signal is LOW for 750 microseconds during each period. **d)** The frequency of the PWM signal is 25 kHz.

Q4. A microcontroller is communicating with a peripheral using SPI at a clock frequency of 4 MHz. If the data frame size is 8 bits, how long will it take to transmit a single byte of data?
a) 0.25 microseconds **b)** 2 microseconds **c)** 0.5 microseconds **d)** 1 microsecond

Q5. Which of the following best describes the clock behavior in asynchronous communication?
(a) The clock is shared between sender and receiver. **b)** The clock is required internally by each device but not transmitted between devices. *(c) Timing between the sender and receiver is maintained through baud rate and start/stop bits.* **(d)** *Asynchronous communication relies on an external clock for synchronization.*

SECTION-II [10 MARKS]

Carry TWO mark each. No Negative Marking

Q6. *The system uses an interrupt to handle a sensor that generates an interrupt every 2 milliseconds. If the interrupt service routine (ISR) takes 50 microseconds to execute.*

(a) The time available for other tasks between interrupts is _____**microseconds.**
(b) Is the system can handle up to 20,000 interruptions per second? Justify the reason for your answer
(c) The total time used by interrupts is _____% of the processor time.
(d) is system can handle up to 10,000 interrupts per second without losing data? Justify the reason for your answer

Q7. A microcontroller polls a sensor every 200 microseconds. Each polling operation takes 25 microseconds. If the sensor generates data every 2 milliseconds.

a) The CPU spends _____% of its time polling the sensor.
b) The percentage of time the CPU is idle (not polling) is _____%.
c) The total number of polling operations in 1 second is _____.
d) The time wasted in polling (when no new data is available) is _____% of the polling period.

Q8. An I2C bus operates at 400 kHz (Fast Mode) and transmits a 20-byte message, including a 1-byte address, without any delay between bytes. Which of the following is correct?
a) The total transmission time is 3.78 milliseconds. **b)** Each byte transfer includes 8 data bits and 1 acknowledgment bit. **c)** The total number of clock cycles required for the transmission is 189. **d)** The total transmission time is 0.45 ms.

Q9. Imagine a system where a microcontroller needs to read temperature data from a sensor every second and display it on an LCD screen. Compare how this can be done using polling versus interrupts.

Q10. Explain the sequence of steps (9 steps) that occur when an interrupt (in ARM Microprocessor) is triggered in an embedded system, starting from detecting the interrupt to resuming the main program.

SECTION-III [10 MARKS]

Carry **2.0** mark each. **+1** Negative Marking for wrong answer

Q11. Which of the following are correct about the analog output voltage (V0) and its implications?

```
#include "mbed.h"
AnalogOut output(PA_0);
int main() {
  while (true) {
    output = 0.25;  ThisThread::sleep_for(500ms);  output = 0.75;  ThisThread::sleep_for(500ms);
  }
}
```

(a) The V0 will oscillate between 0.825V and 2.475V if the reference voltage is 3.3V. **(b)** The V0 will oscillate between 0.825V and 2.475V if the reference voltage is 5V. **(c)** The V0 will oscillate between 0.825V and 2.475V if the reference voltage is 2.5V. **(d)** The V0 will oscillate between 0.825V and 2.475V if the reference voltage is 1.65V.

Q12. Review the following code that uses an analog input to control an LED via PWM. What can be inferred about the behavior of the LED and the analog input?

```
#include "mbed.h"
AnalogIn analogInput(A0);
PwmOut led(PA_2);
int main() {
  led.period(0.01);
  while (true) {
    float value = analogInput.read();
    led.pulsewidth(value * 0.01);
    ThisThread::sleep_for(100ms);
  }
}
```

Options:

a) The LED brightness will vary linearly with the analog input value, ranging from 0% to 100% brightness.
b) The LED brightness will oscillate between maximum and minimum values every 100 milliseconds.
c) The PWM period is 10 ms, so the LED brightness will change in increments proportional to the analog input value.
d) The LED brightness will be directly proportional to the analog input value with a period of 10 ms.

Q13.

```
#include "mbed.h"
Spi spi(p5, p6, p7); // MOSI, MISO, SCK
DigitalOut cs(p8);
int main () {
spi.format(8, 0);  spi.frequency(1000000);  cs = 0;  spi.write(0xAA); cs = 1;
}
```

From the above given code, which of the following sequences of function calls would lead to successful data transmission in an SPI system with multiple slave devices?

(a) cs1 = 0; spi.write(0xAA); cs1 = 1; cs2 = 0; spi.write(0xBB); cs2 = 1; **(b)** spi.write(0xAA); spi.write(0xBB); cs1 = 0; cs1 = 1;
(c) cs1 = 0; spi.write(0xAA); cs2 = 0; spi.write(0xBB); cs2 = 1; cs1 = 1; **(d)** cs1 = 0; spi.write(0xAA); cs1 = 1;

Q14.

```
#include "mbed.h"
I2C i2c_master(p9, p10);
const int SLAVE_ADDR = 0x42 << 1;
void send_data(int data) {
  char cmd[2];  cmd[0] = 0x00;  cmd[1] = data;
  i2c_master.write(SLAVE_ADDR, cmd, 2);
}
int main() {
  i2c_master.frequency(100000);
  while (true) {
    send_data(123);  ThisThread::sleep_for(2s);
  }}
```

Now If i2c_master.frequency(100000); is replaced with i2c_master.frequency(10000);, what effects can be expected? (Select all that apply)

(a) Data transmission will be significantly slower, resulting in a longer execution time for the loop.
(b) The communication might fail altogether if the slave device cannot handle lower frequencies.
(c) The longer wait time for the slave to process each command may improve data integrity.
(d) The change will have no effect on data transmission, as I2C devices are generally tolerant of different frequencies.

Q15. For ARM Cortex-M Microcontroller Scenario: We have an ARM Cortex-M microcontroller with three interrupt sources: Priority order of Interrupts is X>Y>Z and Interrupt X occurs at T = 0 ms ; Interrupt Y occurs at T = 1 ms ; Interrupt Z occurs at T = 2 ms. Flag Setting: =1 µs; Context Saving: = 2 µs; Context Restoring:=2 µs; Interrupt 'X' ISR:= 8 ms; Interrupt 'Y' ISR:= 5 ms; Interrupt 'Z' ISR:= 3 ms ; Interrupt Masking Time: =2 ms (Select all that apply)

(a) Total Latency of Interrupt X< Interrupt Y< Interrupt Z **(b)** Total Latency of Interrupt X> Interrupt Y> Interrupt Z **(c)** Finish Handling of Interrupt X = Start Handling of Interrupt Y & Finish Handling of Interrupt Z =15 ms **(d)** None of above

Rajiv Gandhi Institute of Petroleum Technology, Jais, Amethi
B. Tech CSE/IT/CSD/MC/IDD Mid Semester Examination 2024 – 25
Subject: CS341 Advance Algorithms

Time 2 hrs Full Marks 30

Note: Attempt all questions. The marks of the questions are provided along with the questions. You need to explain your answers.

1. Solve the following recurrence relations.
   (a) $T(n) = 4T(n/3) + n \log n$ [2]
   (b) $T(n) = 3T(n/4) + n \log n$ [2]

2. Arrange the following functions in increasing order of their asymptotic time complexity:
   $f_1(n) = n!$, $f_2(n) = n \log n$, $f_3(n) = \frac{n^2}{\log n}$, $f_4(n) = 2^n$,
   $f_5(n) = n^{1.5}$, $f_6(n) = \log^2 n$ [2]

3. Why we cannot get the optimal solution to $0-1$ knapsack problem using greedy algorithm. Justify. [2]

4. To find the maximum spanning tree of a graph, that is, the spanning tree of largest total weight: we multiply all the edge weights by 1 and then find the minimum spanning tree by any of the standard algorithms. This will give a maximum spanning tree. State Yes or No with reasoning. [2]

5. In merge sort to sort an array of size N, we divide the array into two sub-arrays, sort these two sub-arrays recursively, and then merge them. Let us assume a modified merge sort where instead of dividing the array into two, we are dividing it into four sub-arrays, sorting each sub-arrays recursively and then merging them. Obtain the time complexity of this modified merge sort. [3]

6. Consider there are N positive integers that are stored in an array. We want to sort this array in ascending order using Quick Sort. Assume the median element is selected as a pivot in Quick Sort each time. Let the time complexity to find the median element in an array of size N be $\mathcal{O}(N \log N)$. Compute the time complexity of this type of Quick sort.

7. For the sequence $[10, 22, 9, 33, 21, 50, 41, 60, 80]$, find the length of the longest increasing subsequence. Provide the steps of your algorithm and analyze its time complexity. For example, $[21, 50, 60]$ is one such increasing sub-sequence of length 3. Your objective is to find the longest such sub-sequence.

8. Kruskal's algorithm to find the Minimum Spanning Tree is greedy in nature. However, not all greedy algorithms are optimal. Why the Kruskal algorithm is optimal?

9. You are given an array of non-negative integers, where each element represents the height of a column of width 1. After it rains, the goal is to determine how much water can be trapped between these columns. Water is trapped in the dips between taller columns, but no water can be stored on or beyond the first and last columns. For example, you have an array as $[3, 0, 1, 0, 4, 1, 2]$, and the collected rainwater for this array can be visualized in Figure 1.

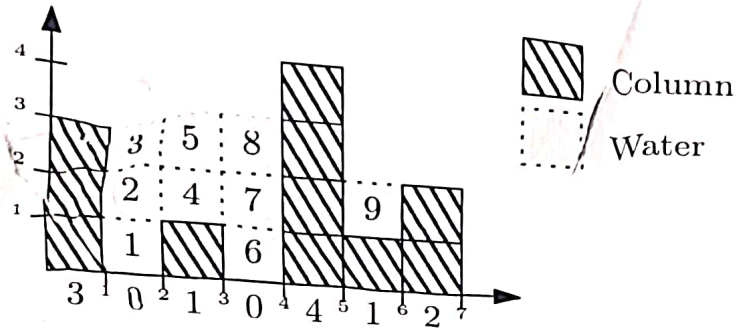


Figure 1: Rain water problem visualization for array $[3, 0, 1, 0, 4, 1, 2]$.

The collected rain water in the above question is 9 units. Now do the following:

(a) **Design a Greedy Algorithm:** Create an efficient algorithm to calculate the total trapped water. [1]

(b) **Proof of Correctness:** Justify your approach using optimal substructure and greedy choice properties. [1]

(c) **Time Complexity:** Analyze your algorithm's efficiency. [1]

(d) **Edge Cases:** Consider cases like all zero heights, strictly increasing or decreasing heights. [1]

10. You are given a 2D grid (matrix) of size $m \times n$, where each cell contains a non-negative integer representing the cost to step on that cell. You start at the top-left corner of the grid (at cell $(0, 0)$) and want to reach the bottom-right corner (at cell $(m-1, n-1)$). From any cell, you can only move **right** *or* ***down***.

Your task is to find *the minimum cost to reach the bottom-right corner from the top-left corner using a dynamic programming-based approach. Also, analyze the time and space complexity of your approach.*

For example: *we have a* 3×3 *matrix as:*

$$\text{Grid} = \begin{bmatrix} 1 & 3 & 1 \\ 1 & 5 & 1 \\ 4 & 2 & 1 \end{bmatrix}$$

Output: *The path with the minimum cost is* $1 \to 3 \to 1 \to 1 \to 1$, *and the total cost is 7.* [3+

22CS3039
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RAJIV GANDHI INSTITUTE OF PETROLEUM TECHNOLOGY, JAIS AMETHI
B.Tech. 3rd YEAR (CSE, IT, MnC, CSD, IDD)
MID-SEM EXAMINATION, September 2024

INSTRUCTOR: Dr. NIRBHAY TAGORE

COURSE CODE: CS231
FULL MARKS: 20

SUBJECT: OPERATING SYSTEMS (OS)
DATE & TIME: 25th September 2024, 12:00 P.M. – 2:00 P.M.

INSTRUCTIONS:

I. All the sections are compulsory. Intermediate choices are given in the section itself.
II. Marks against each question are indicated.
III. Attempt the questions in serial order (if possible).

Section-I

Q1. *Discuss the working principle of HRRN and SJF (in short)? How these two are related to each other with respect to response ratio.* **Marks: 1**

Q2. *Consider three processes P0, P1, P2 and three semaphores a, b, and c. The semaphores are initialized to a=1, b=0, c=0.*

P0	P1	P2
Wait(a); Print "Hello"; Signal(b);	Wait(b); Print "World"; Signal(c);	Wait(b); Print "Command"; Signal(c);

Analyze the given arrangement and tell what are the possible and not possible print statements after successful execution of all the processes? **Marks: 2**

Q3. Write short Note on the following: (Attempt any 4) **Marks: 1*4 = 4**

a) Microkernel and Monolithic Kernel with diagram
b) Is starvation a problem that can happen in priority scheduling? explain how and discuss the solution for that.
c) Convoy Effect with example
d) Difference between 5 and 7 state Process state life cycle with diagram
e) Race Condition in critical section with proper example

Q4. What do you understand from Deadlock? What are the necessary conditions for the deadlock to occur, explain in brief? (2 Marks)

For the given below arrangement apply the Deadlock Avoidance algorithm for multi-instance resources (Total Instances of R1, R2 and R3 are 10, 5, 5 respectively) to check whether there exists any safe sequence

or not. If the safe sequence exists, then write any one of the safe sequences and if it doesn't exist then justify your answer. (3 Marks) **Marks: 2+3 = 5**

	Max Requirement			Current Allocation		
Process	**R1**	**R2**	**R3**	**R1**	**R2**	**R3**
A	7	5	3	1	1	2
B	3	2	2	2	0	0
C	9	0	2	3	0	2
D	2	2	2	2	1	1

Section-II

Q5. Consider a system with four processes P1, P2, P3, and P4 arriving at the same time and with their execution time 'a', 'b', 'c', and 'd', where a<b<c<d. Compare Average Turnaround time (TAT) when SJF Non-pre-emptive and SJF Pre-emptive i.e., SRTF CPU scheduling is used. **Marks: 2**

Q6. For the below-given arrangement:

Consider the scenario that if the process is arriving till t=5 unit time then it will be assigned with Round Robin with TQ=3, while after t=5 unit time the OS will apply Round Robin TQ=5 to all the processes present in the ready queue at t=5.

Tell about the status of ready queue at t=6 and calculate for the average turnaround time and average waiting time after complete execution. **Marks: 3**

Process Id	A.T.	B.T.	Priority
A	0	5	3
B	2	6	1
C	4	4	2
D	6	10	4
E	8	8	1

Q7. Peterson Solution solves the problem of two process synchronization problems by ensuring the mandatory properties. Discuss the mandatory properties, 2 process synchronization problem, and solution in detail with pseudo code for the solution.

Or

Discuss the Reader Write problem in process synchronization along with the solution and pseudocode for the solution. **Marks: 3**