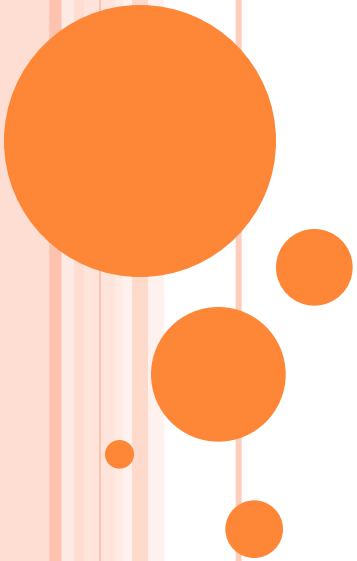
COMPUTER ORGANIZATION AND ARCHITECTURE

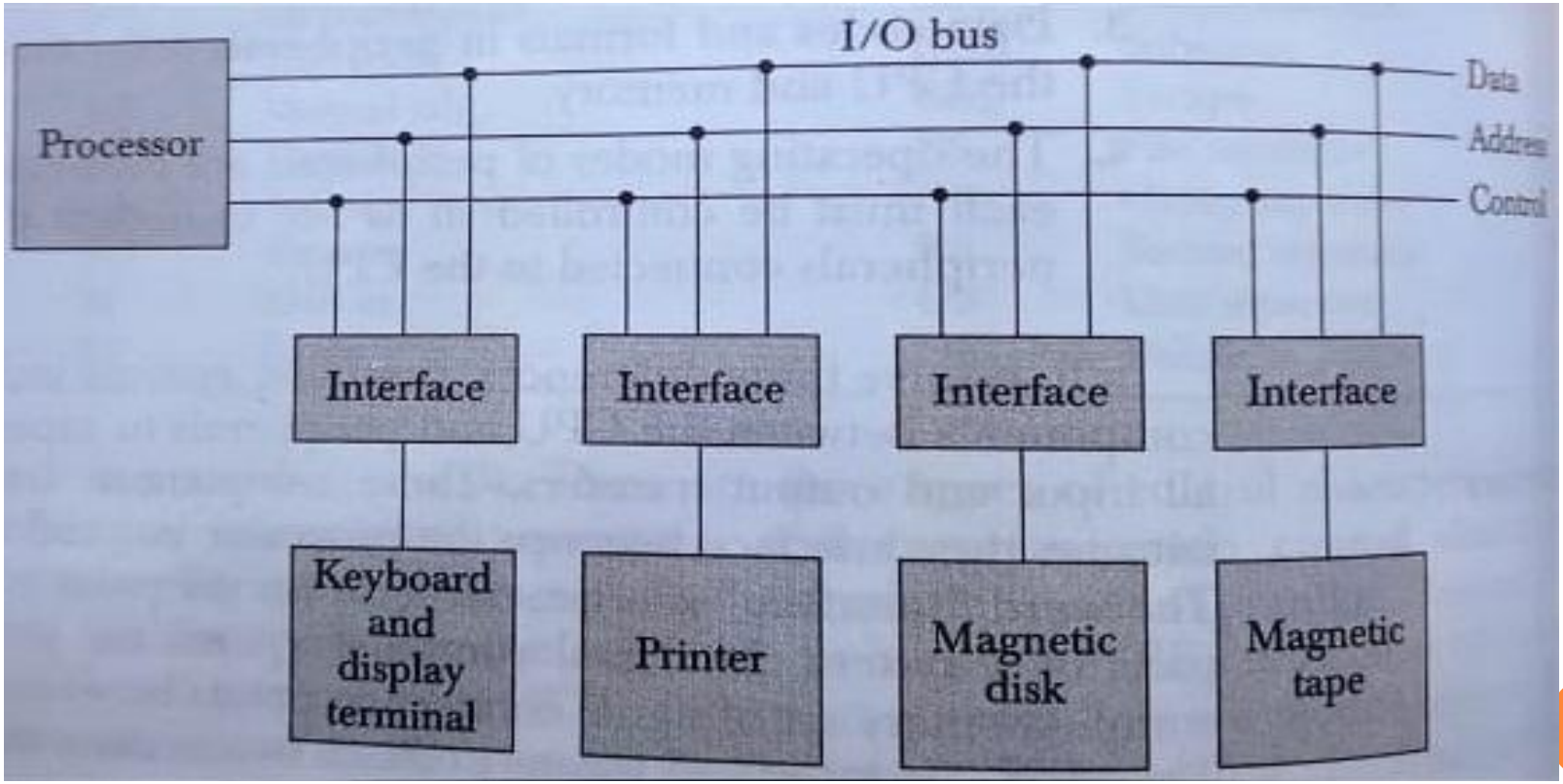
5. Input Output Management



Peripheral devices:

Interface

Speed and Format:
Physical orientation and signal conversion:



Interrupt

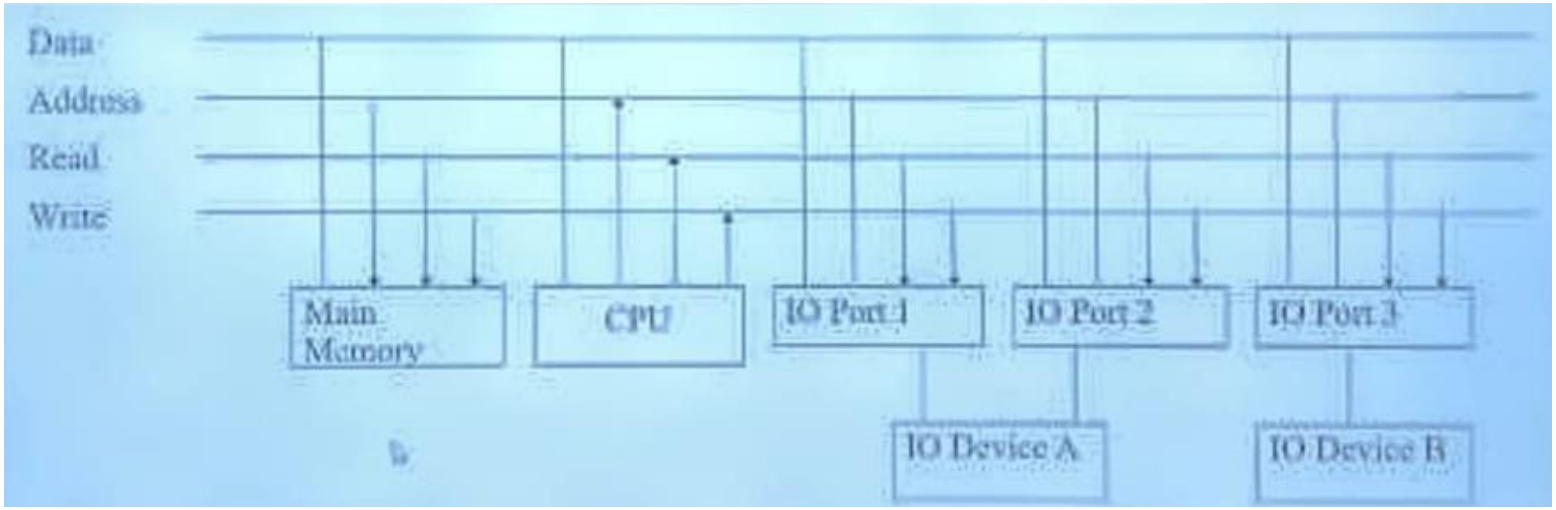
Signal from hardware device to get the processor attention.

- Polled Interrupt (regular check from processor)
- Vectored Interrupt (direct ask from I/O to processor)

How CPU deals with Memory and I/O

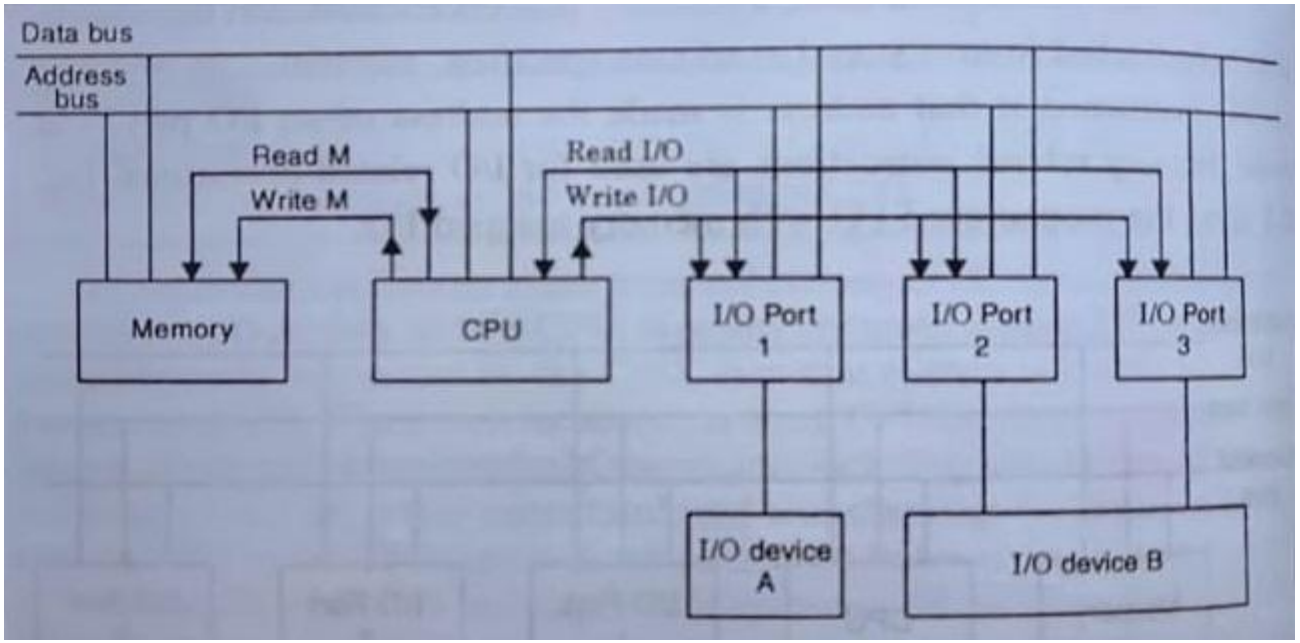
- Memory Mapped I/O:

No separate I/O instructions. Here CPU can use memory type instructions for I/O data. Eg: 8085



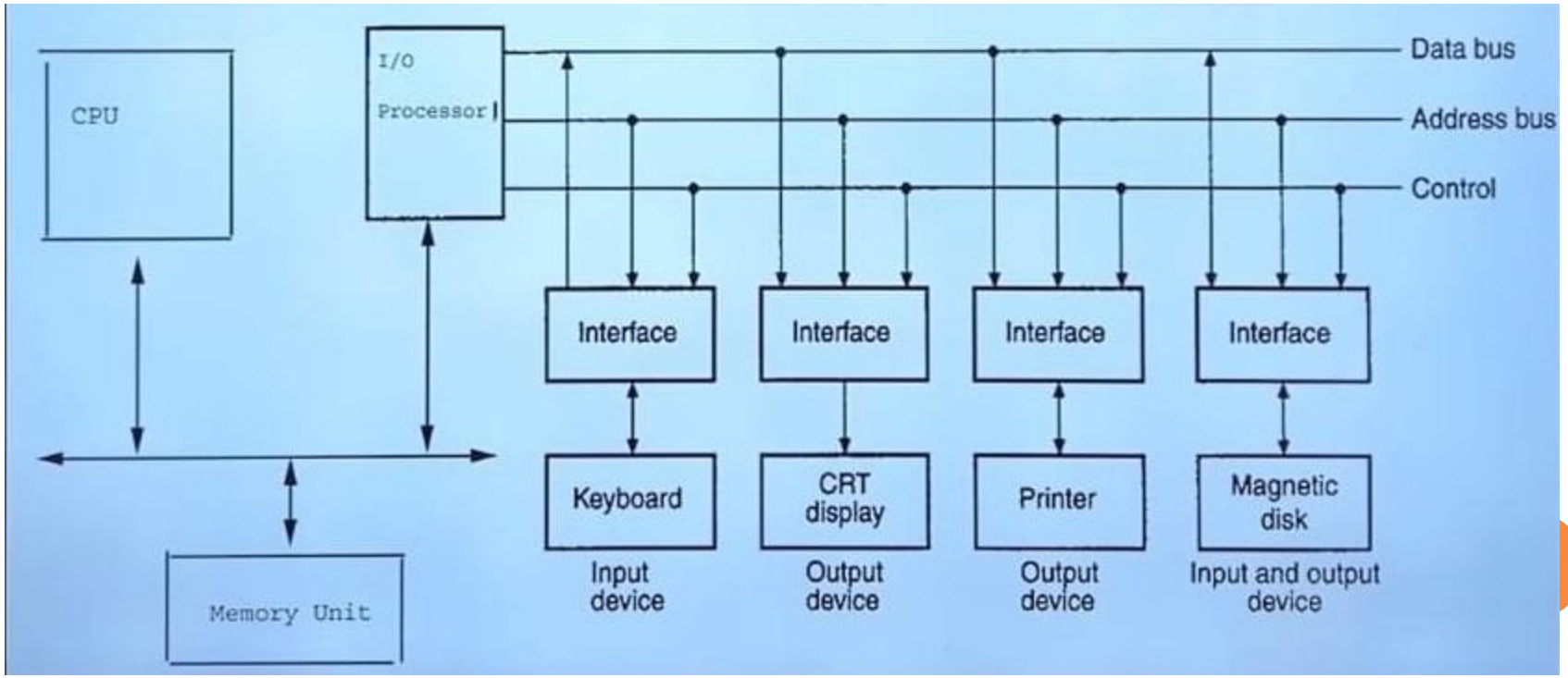
- Isolated I/O:

Separate read write line. I/O read and I/O write are enabled during I/O transfer, same is for memory.
Eg: 8086



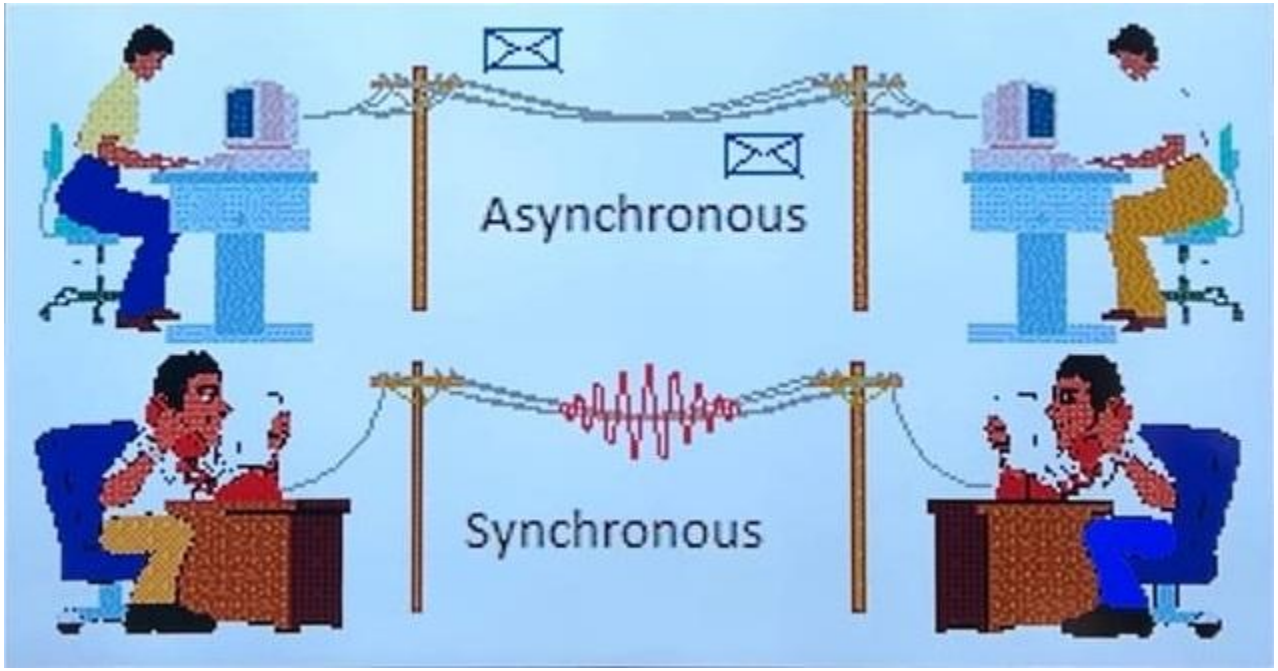
- I/O Processor:

Independent set of address, data and control bus, one for memory and other for i/o. Separate i/o processor than CPU. Purpose of i/o proc. is to provide independent pathway for the transfer of info. between external devices and internal m/y



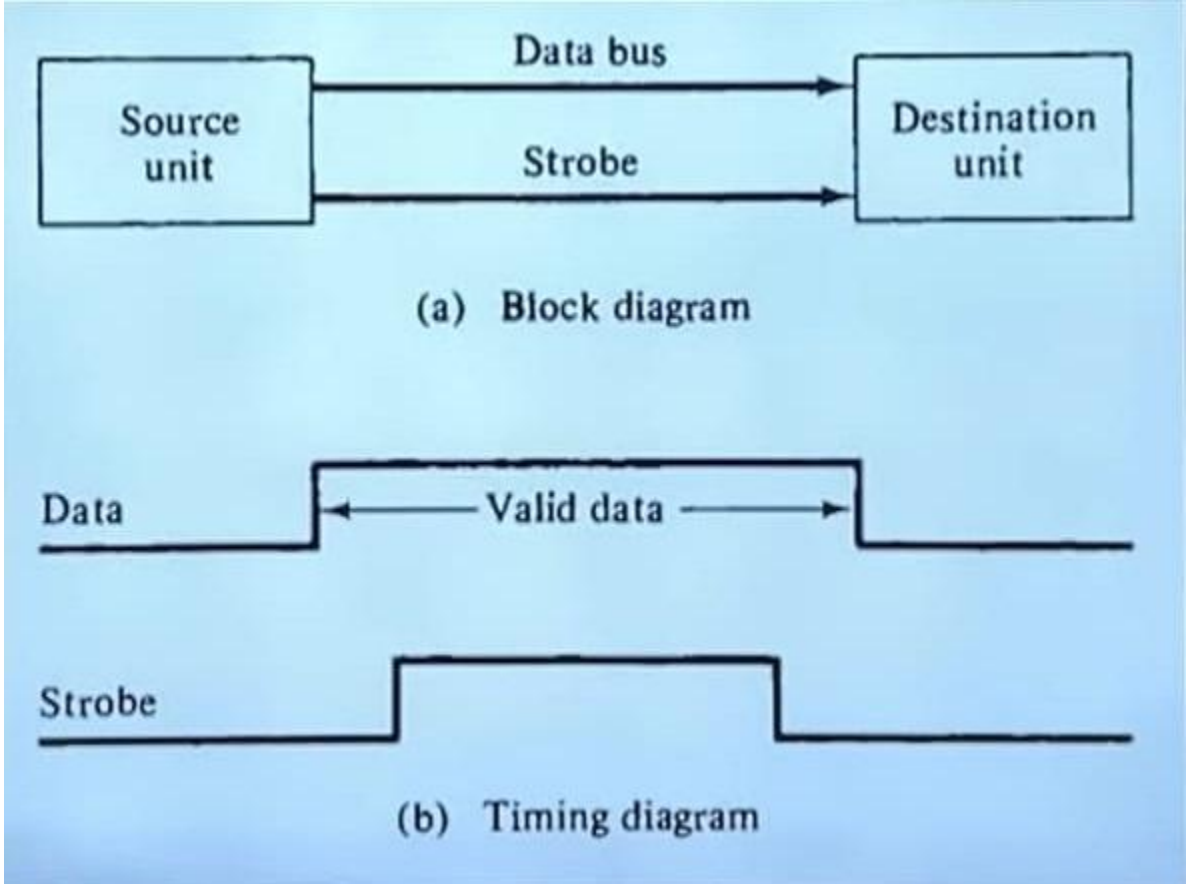
Synchronous vs Asynchronous data Transfer

- Synchronous is achieved by device called master generator (generates periodic clock).

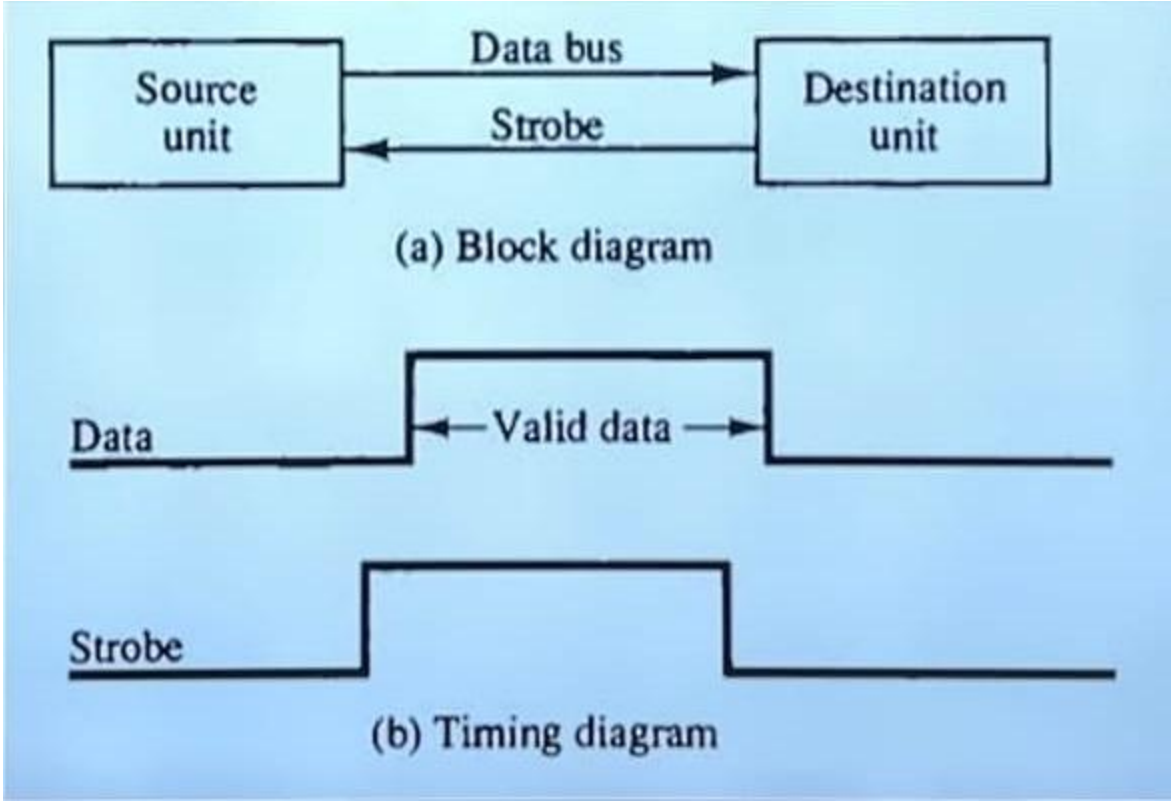


Source Initiated I/O

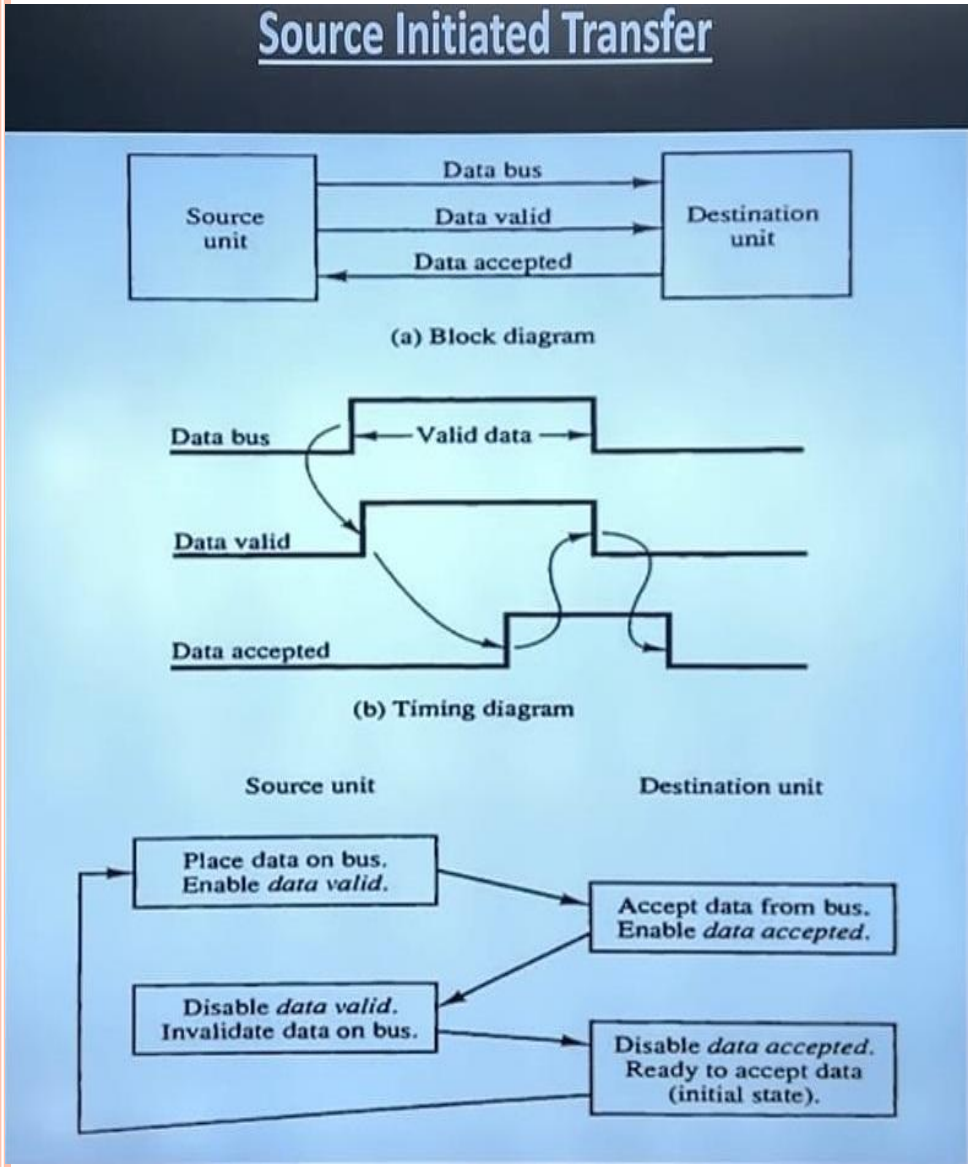
- Strobe pulse methods and handshaking method

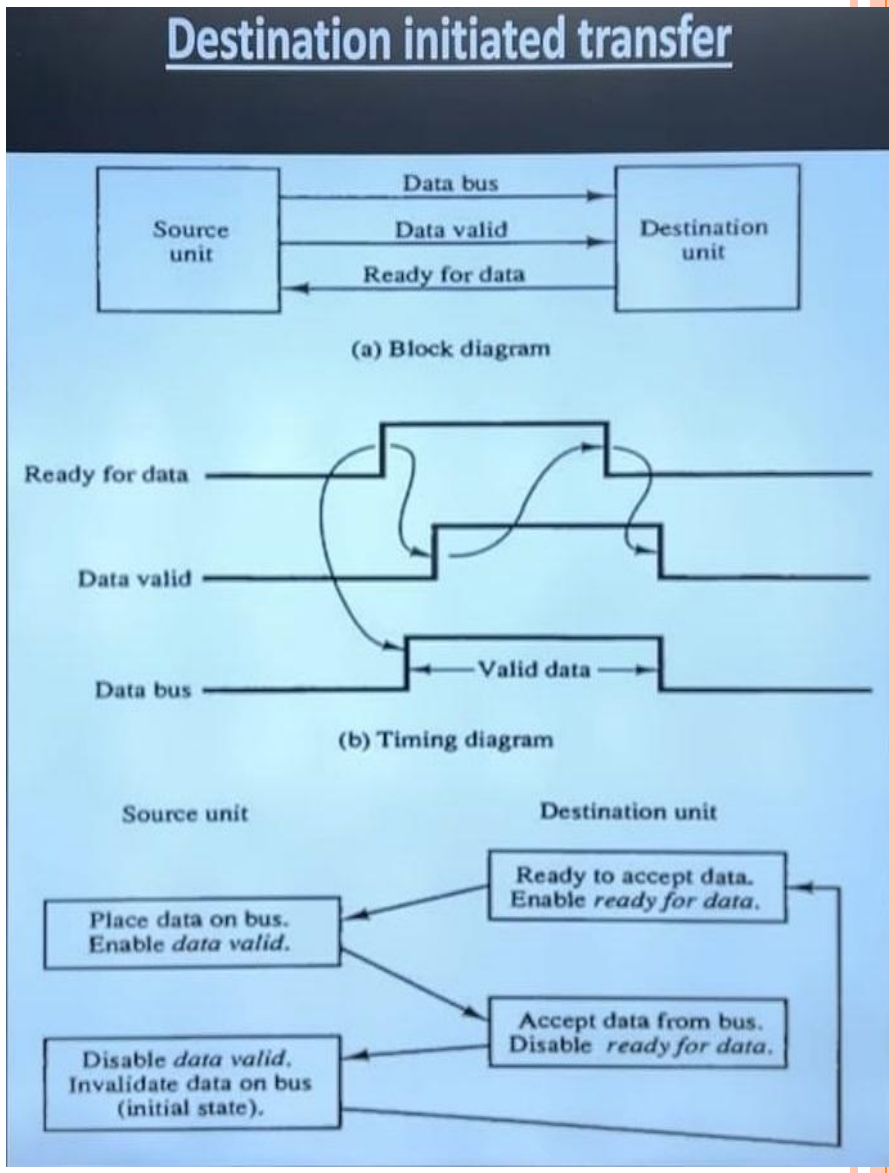


Destination Initiated I/O



❖ **Three-way handshaking**

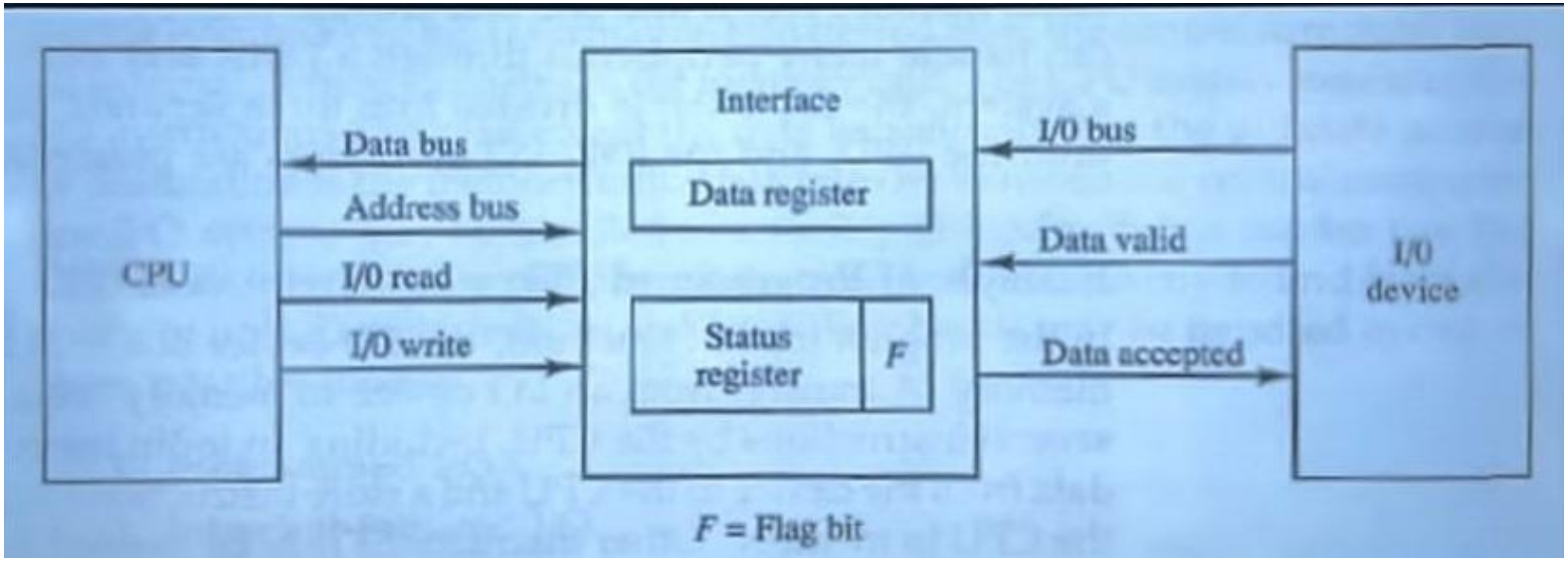


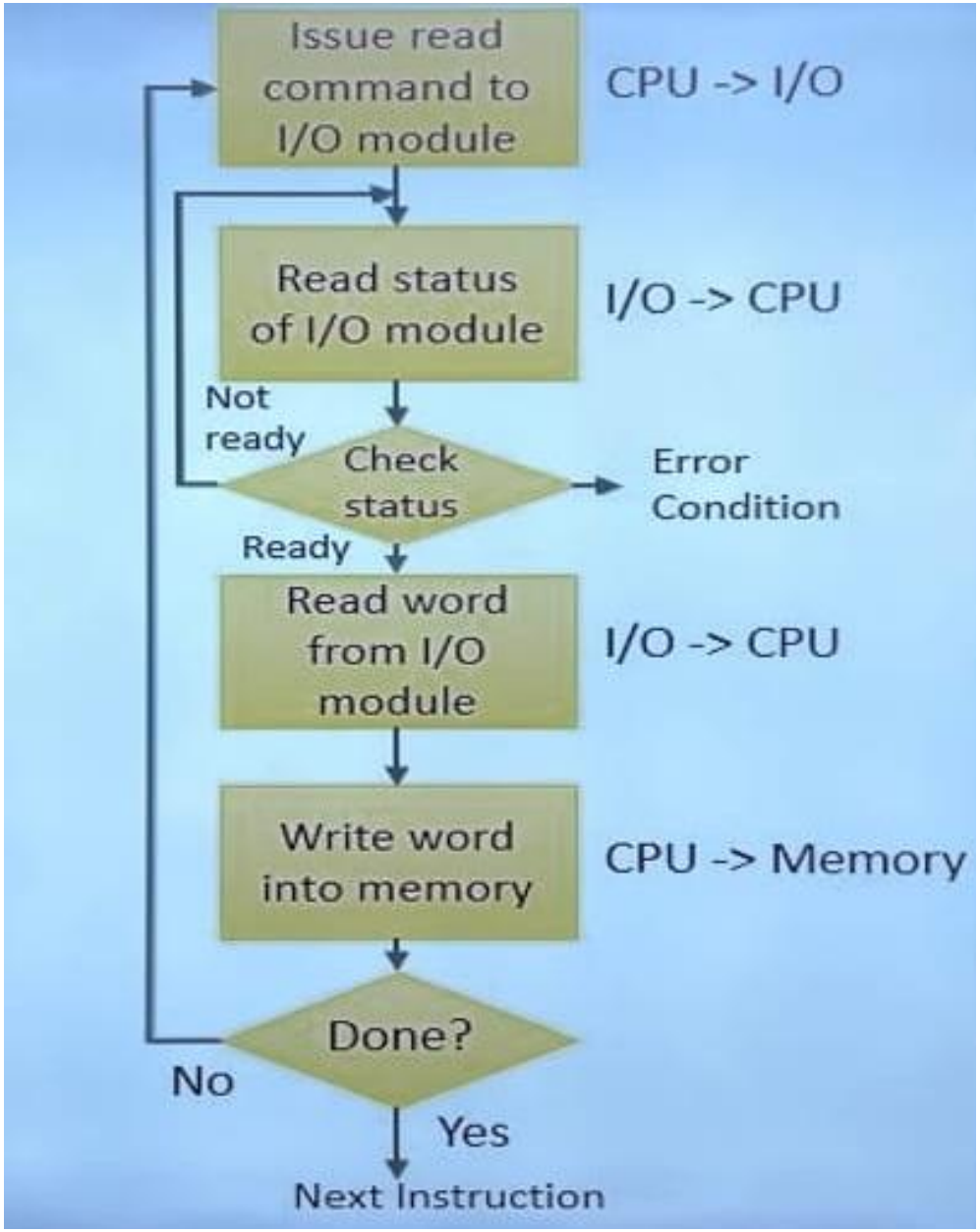


Modes of Data Transfer

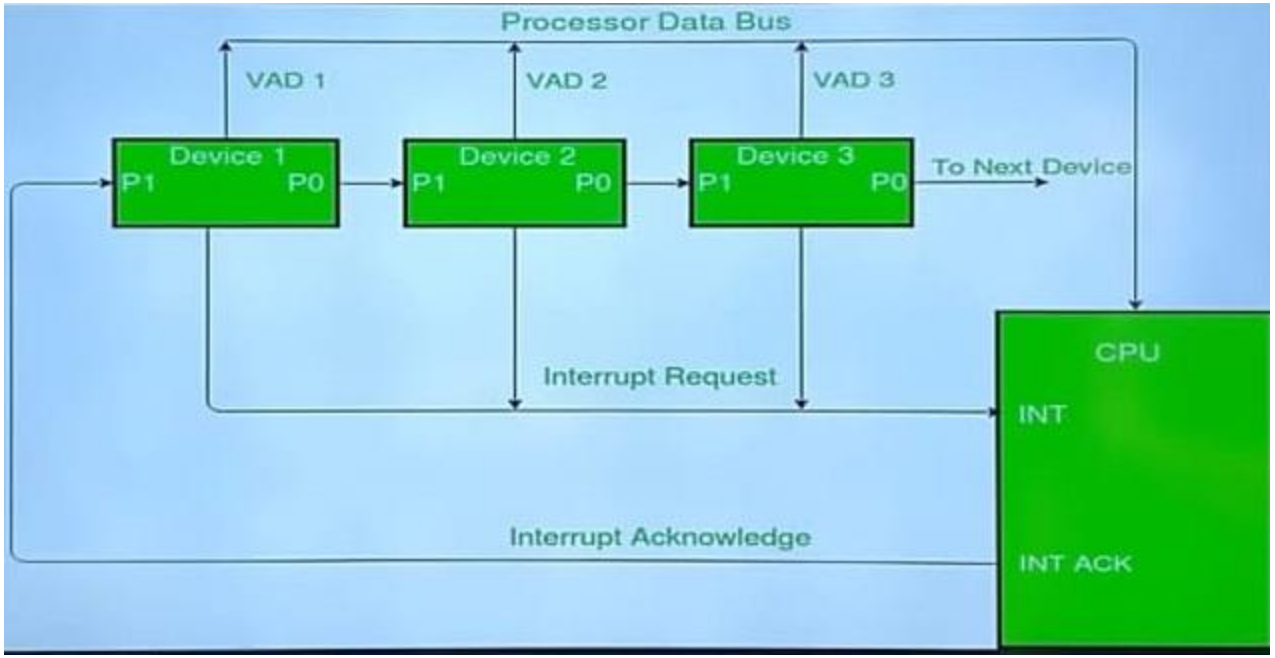
- Programmed I/o
- Interrupt Initiated I/O
- DMA

Programmed I/O




Issue read command to I/O module
CPU -> I/O
Read status of I/O module
I/O -> CPU
Not ready
Check status
Error Condition
Ready
Read word from I/O module
I/O -> CPU
Write word into memory
CPU -> Memory
Done?
No
Yes
Next Instruction

Interrupt Initiated I/O

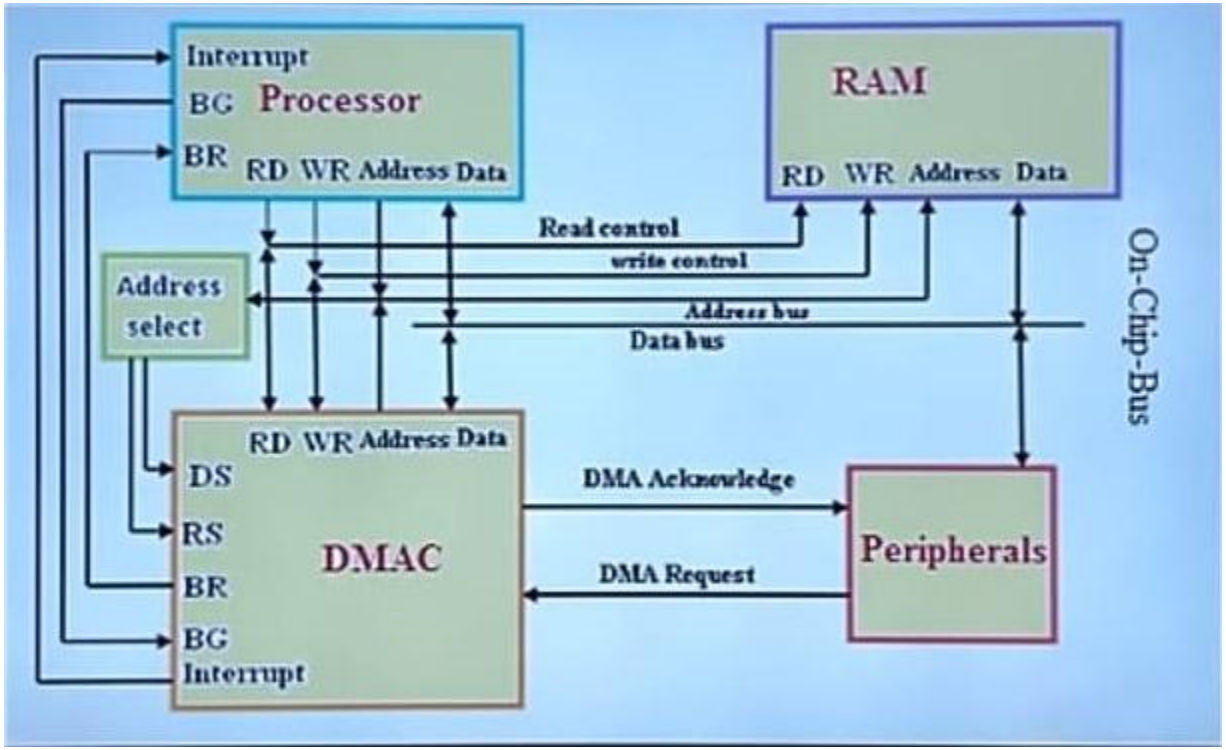


Non-vectored and vectored interrupt

Kinds of Interrupt

- Hardware Interrupt
- Software Interrupt
- Maskable Interrupt (Optional)
- Non-Maskable Interrupt (High priority demands)

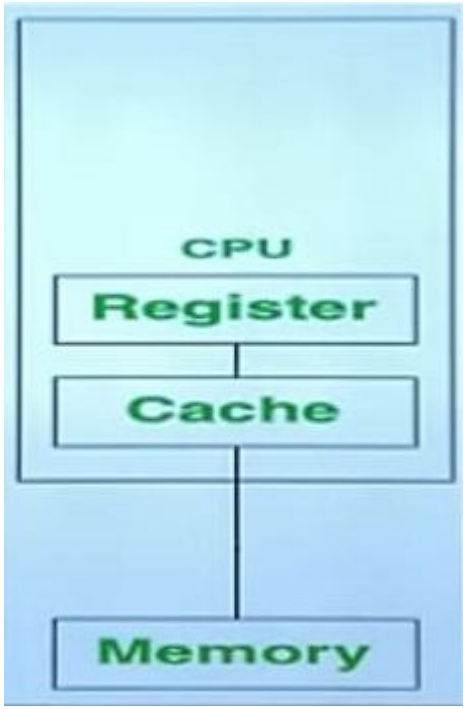
DMA (Direct M/y Access)

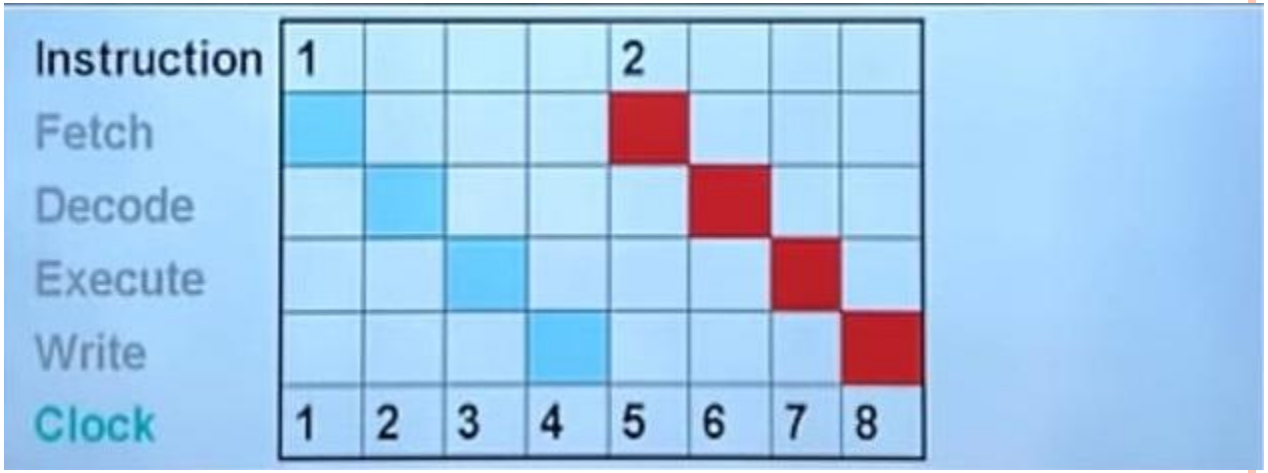


- Burst Mode and Cycle stealing mode

Pipelining (Intro):

- Uni-processing Systems





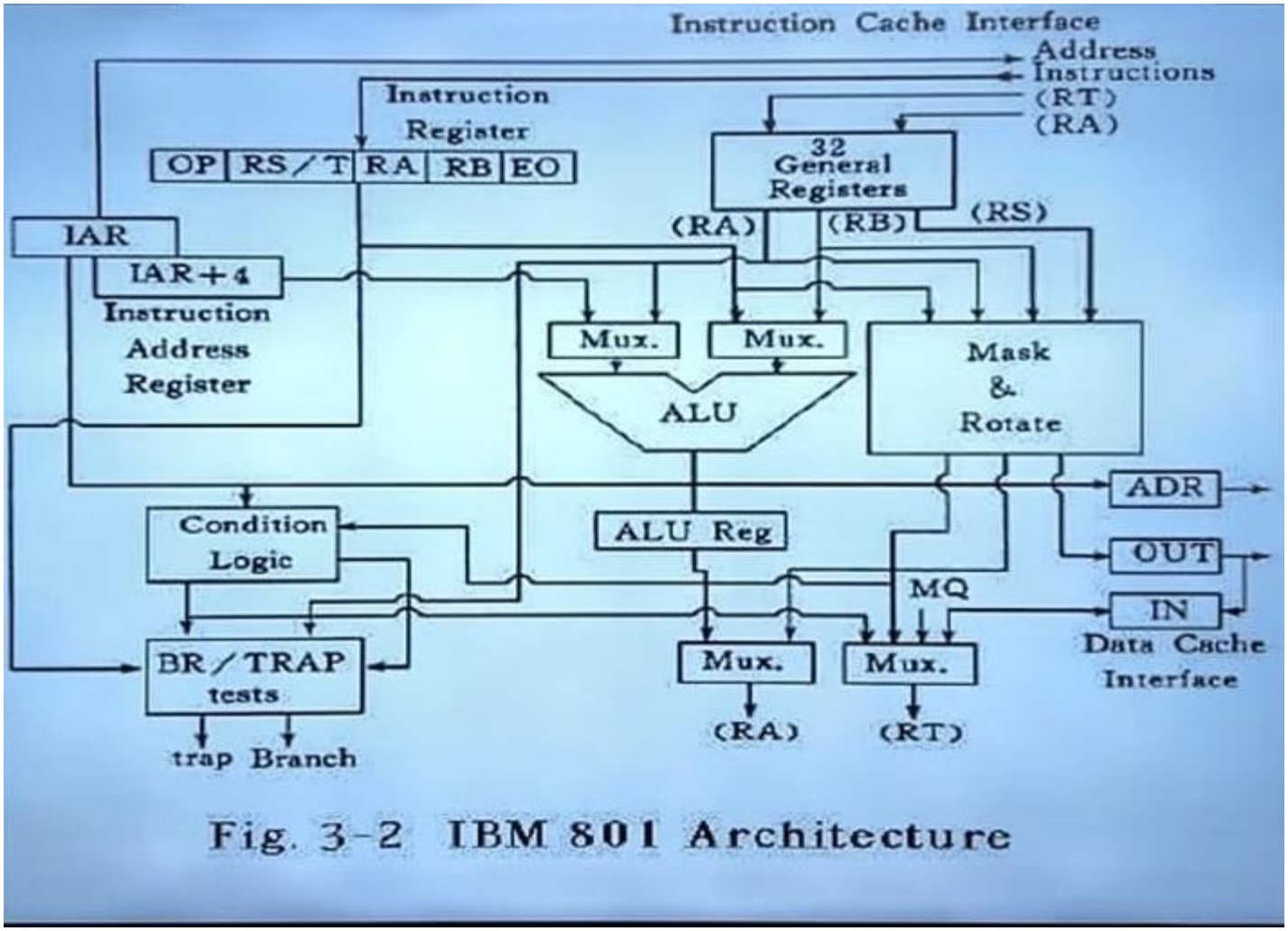
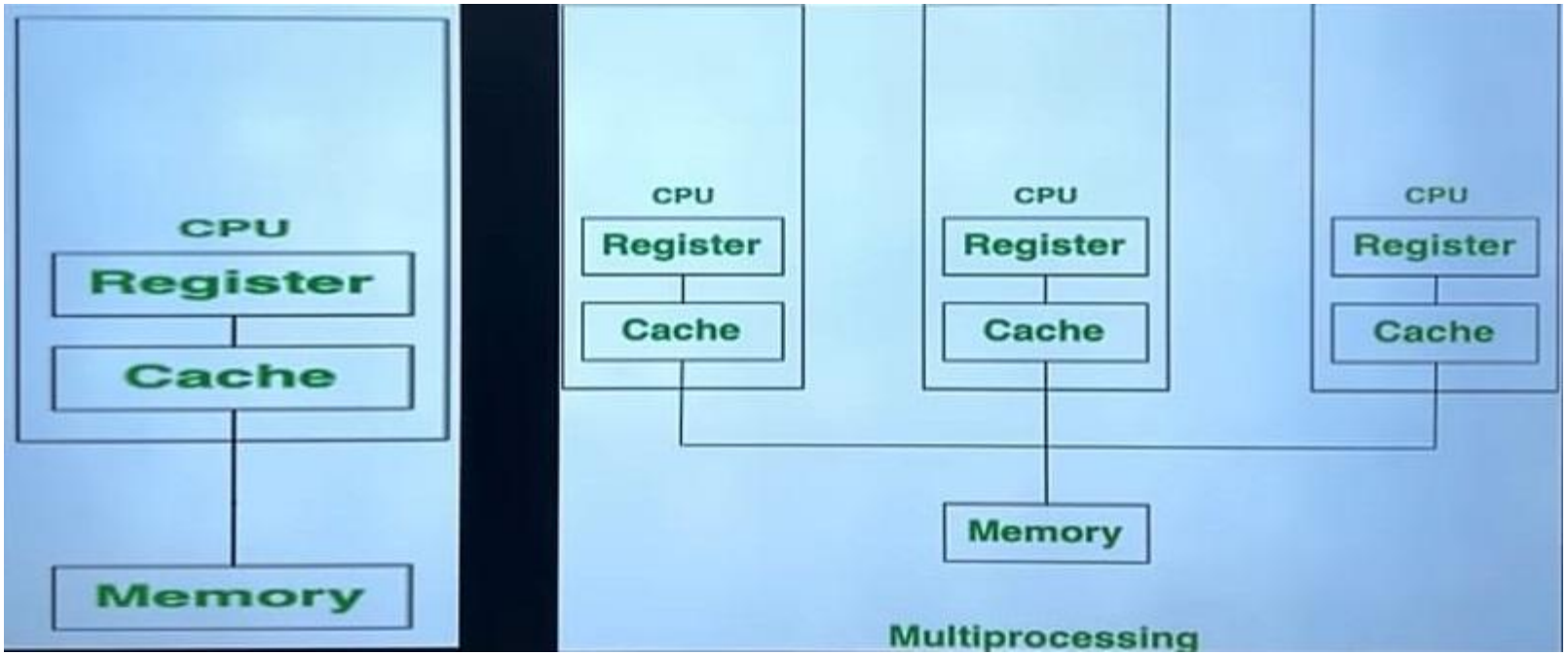


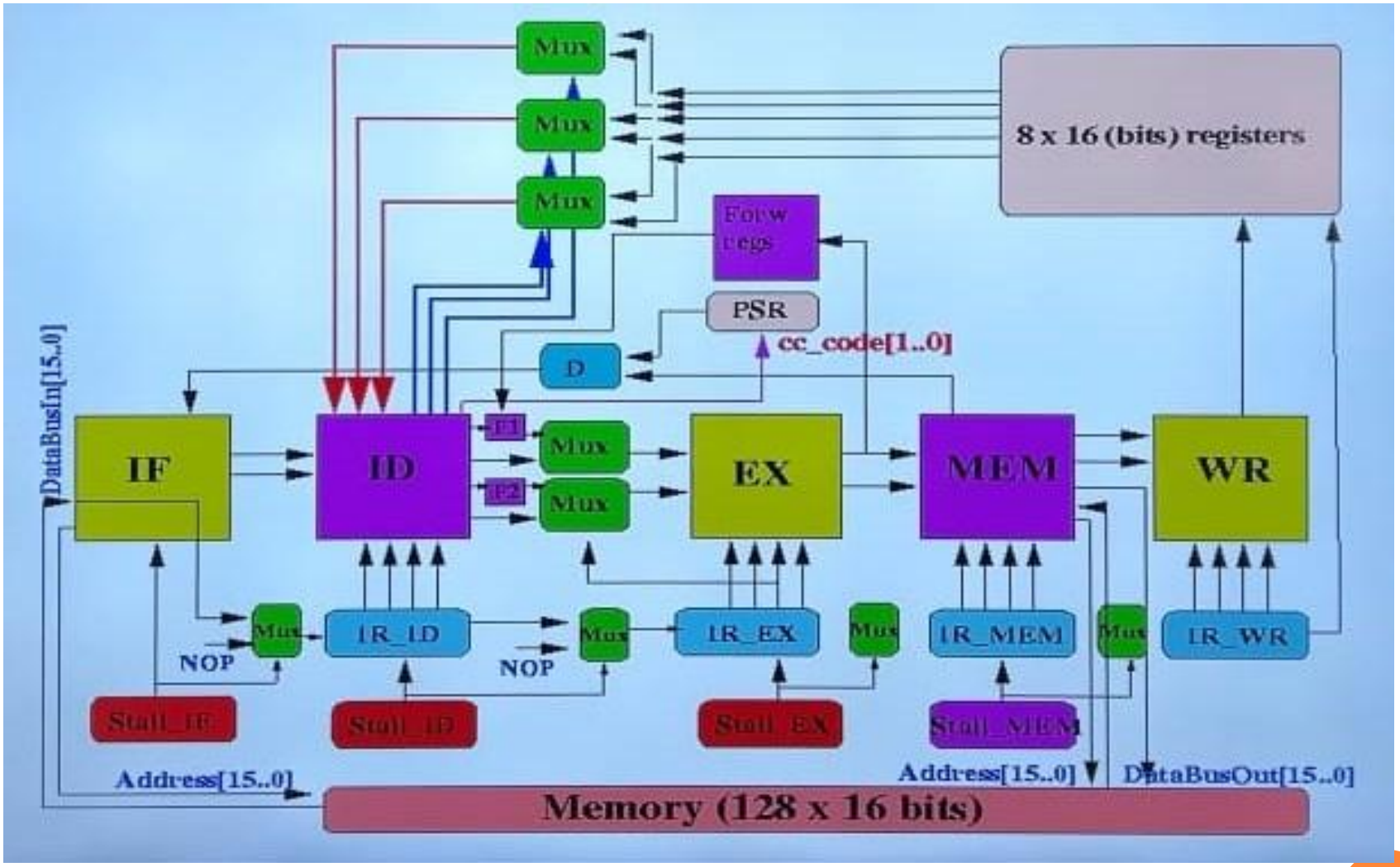
Fig. 3-2 IBM 801 Architecture

- Uni-processing vs Multi-processing Systems



Pipelining:

- Pipelining is a phenomenon or method using which, we will be able to run more than one instruction at the same time, on a single processor.


Mux
Mux
Mux
8 x 16 (bits) registers
Forw regs
PSR
cc_code[1..0]
D
DataBusIn[15..0]
IF
ID
F1
F2
Mux
Mux
EX
MEM
WR
Mux
IR_ID
Mux
IR_EX
Mux
IR_MEM
Mux
IR_WR
NOP
NOP
Stall_IF
Stall_ID
Stall_EX
Stall_MEM
Address[15..0]
Address[15..0]
DataBusOut[15..0]
Memory (128 x 16 bits)

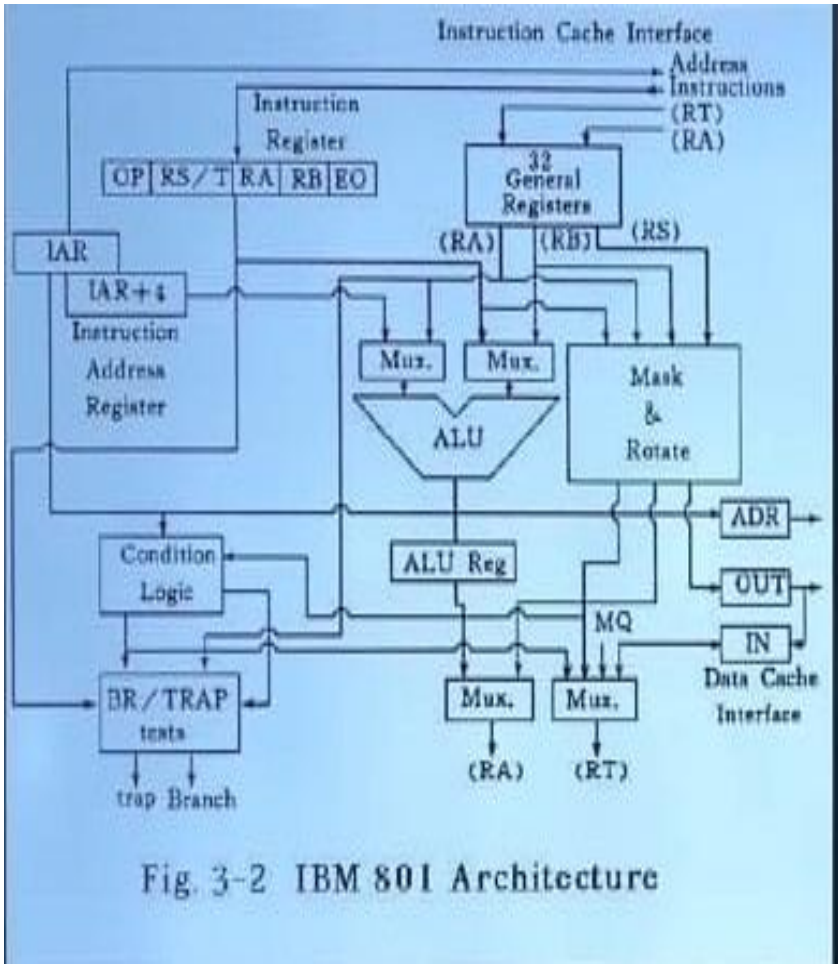
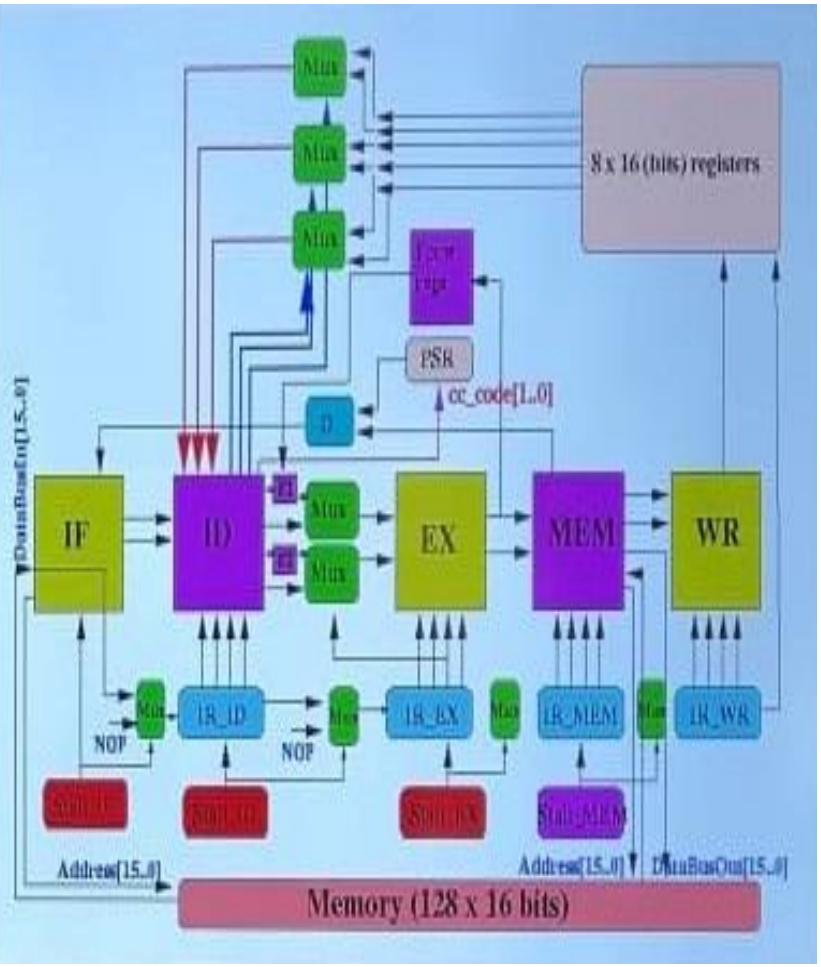
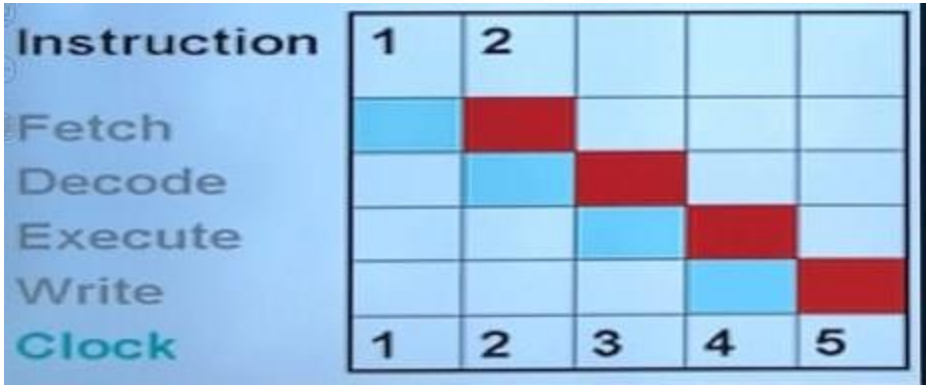


Fig. 3-2 IBM 801 Architecture



❖ **Uni, Multi, and Pipelined processor working**



Pipelining in Depth:

- Without Pipelining
- With pipelining
- CPI (Clock Per Instruction)
- Speedup, Efficiency

Q Consider a system where clock is triggering at a speed of 1MHz (1 clock = 1 μs) In a pipelined processor there are 4 stages and each stage take only 1 clock, if a program has 10 instruction then it will take what time?

- On a non-pipelined processor

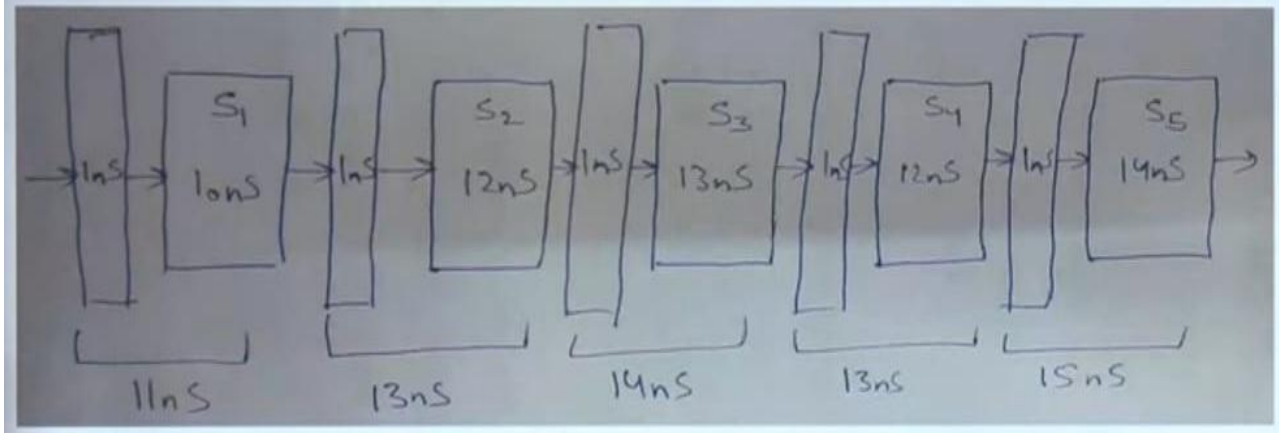
	1	2	3	4	5	6	7	8	9	10	11	12	13
IF	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}			
ID		I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}		
EX			I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	
WB				I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}

Q Consider 5 instruction with following clock requirement?

	F	D	E	WB
I_1	1	2	1	1
I_2	1	2	2	1
I_3	2	1	3	2
I_4	1	3	2	1
I_5	1	2	1	2

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
I_1																		
I_2																		
I_3																		
I_4																		
I_5																		

Q After considering this diagram what must be the frequency of the processor to ensure that work of every stage will complete in 1 clock stage wise?



	S_1	S_2	S_3	S_4	S_5
1ns					
2ns					
3ns					
5ns					
15ns					

P_1: Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.

P_2: Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.

P_3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.

P_4: Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.

Which processor has the highest peak clock frequency?

Hazards

- Types of Hazards

Structural Hazards, Control Hazards, Data

Hazards

Q Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution, if 25% of the instructions incur 2 pipeline stall cycles is **(Gate-2014) (2marks)**

Q A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO)and Write Operand (WO)stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions,3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions? **(Gate-2010) (2 Marks)**

Instruction	Meaning of instruction
I_0: MUL R_2, R_0, R_1	$R_2 \neg R_0 * R_1$
I_1: DIV R_5, R_3, R_4	$R_5 \neg R_3 / R_4$
I_2: ADD R_2, R_5, R_2	$R_2 \neg R_5 + R_2$
I_3: SUB R_5, R_2, R_6	$R_5 \neg R_2 - R_6$

(A) 13 **(B)** 15 **(C)** 17 **(D)** 19

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20